HeteroSiC – WASMPE 2009

Catania (Italy), May 6th- 8th , 2009

International workshop on 3C-SiC hetero-epitaxy (HeteroSiC '09)

Catania (Italy), May 6th-7th, 2009

Workshop on Advanced Semiconductor Materials and devices for Power Electronics applications (WASMPE 2009)

Catania (Italy), May 7th-8th, 2009

Edited by : Vito Raineri and Fabrizio Roccaforte

Consiglio Nazionale delle Ricerche
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Preface

This proceedings volume contains the extended abstracts of the contributions presented at the third edition of the international workshop on SiC hetero-epitaxy (HeteroSiC '09) and at the third edition of the Workshop on Advanced Semiconductor Materials and devices for Power Electronics applications (WASMPE 2009) for the first time hold jointly. The two events could take advantage by the MANSIC project mid-term meeting organized close to the workshops and allowing to all project participants to get involved also in these two other events. In particular, HeteroSiC has been also supported by the project while both workshops received an enthusiastic and stimulating adhesion by the entire MANSIC community. The fruitful concomitancy of the events allowed to provide a larger but still well focused forum for scientists and engineers coming from public research institutions and industry and contributing to the particular success of this edition in term of both number of participants (122) and scientific and technical level. In this edition a particular emphasis was directed by the local scientific committee to the participation of industry that indeed is uppermost with respect the past editions illustrating the industrial challenges and presenting some innovative solutions adopted. Also the topics were reviewed with respect past editions including new and innovative trends in the field.
The contributed papers were selected from more than 70 submitted abstracts from over 32 research institutions and 13 industrial research centers in 11 countries all over the world. The futures trends and perspectives in the field have been reviewed focusing on emerging materials, methods and techniques. The two scientific committees for HeteroSiC and WASMPE really made a significant work in suggesting and stimulate referenced scientists to participate and setting an effectual scientific program.
HeteroSiC has appeared has a growing field attracting new topics and promising scientific and technological issues. Onward the traditional topic of 3C-SiC politype on Si an emerging field appeared the growth of cubic silicon carbide (β phase) on the hexagonal politypes (α phase). Particularly, the 3C/4H interface shows a spontaneous polarization and the formation of a two dimensional electron gas opening to SiC extraordinary perspectives. Furthermore, the growth of unstrained 3C on hexagonal SiC allowed the opportunity to have high quality cubic silicon carbide material that can be used even as seed for crystal growth. Free standing 3C-SiC and related homoepitaxy has been faced, too. Already well established is the heteroepitaxial growth of GaN on SiC, particularly interesting for power RF applications but of course driven in the past by optoelectronics applications while very promising come out the formation of graphene on SiC (both 4H- and 3C politypes) opening to several fundamental opportunities and to the industrial fabrication of (nano)sensors and devices.
Power electronics applications seems the most interested industrial application for wide band gap semiconductors, remaining SiC (mainly 4H polytype) the most mature material in terms of crystal quality and wafer dimension. Even if some MEMS and sensor perspectives have been presented during HeteroSiC (mainly interesting SME), the main interest from large companies appears on high efficient power and RF devices. Large diameter SiC wafers and high quality thick layers of GaN on Si are the main challenges for material growth to achieve reliable power devices for industry. Processing related crucial aspects are still mainly related to switches, particular MOSFET and the interface between the gate oxide and SiC. The cost is still the main issue even if the high efficiency of those devices, unreachable with standard semiconductors even using advanced technologies and coming to the general attention for the energetic saving and CO_2 emission limitation rules imposed. Also perspectives and challenges of futures materials such as diamond for power applications have been presented.
The generous support of the sponsors enabled the organizers to keep the conference fee at affordable level, furthermore extending the participation to all local interested researchers.
The great help provided by the organizing committee in setting up the conference is gratefully acknowledged, the generous work of the persons significantly contributed to the success of the meeting and we are particularly grateful to them.

Catania, May 6th, 2009

Vito Raineri
Fabrizio Roccaforte

Scientific Program

Wednesday May 6th 2009

HeteroSiC '09

8:30 **Welcome**

Session 1 **3C-SiC on hexagonal SiC and homoepitaxial**
Chair: Gabriel Ferro *(LMI, Villeurbanne, France)*

8:45-9:00 **Growth and characterization of low doped 3C-SiC layers deposited by VLS technique**
J. Lorenzzi [1], G. Zoulis [2], O. Kim-Hak [1], S. Juillaguet [2], G. Ferro [1] , J. Camassel [2]
[1] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France
[2] GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France

9:00-9:15 **TEM study of 3C-SiC layers grown by sublimation epitaxy on 6H-SiC substrates**
M. Marinova [1], M. Beshkova [2], A. Mantzari [1], M.Syväjärvi [2], R. Yakimova [2], E.K.Polychroniadis [1]
[1] Department of Physics, Aristotle University of Thessaloniki, Greece
[2] Department of Physics, Chemisty and Biology, Linköping University, Sweden

9:15-9:30 **Sublimation epitaxy of 3C-SiC growth and characterization**
M. Beshkova [1], J.C. Lorenzzi [2], N. Jegenyes [2], R. Vasiliaskas [1], J. Birch [1], M.Syväjärvi 1, G. Ferro [2], R. Yakimova [1]
[1] Department of Physics, Chemisty and Biology, Linköping University, Sweden
[2] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France

9:30-9:45 **Rapid thermal oxidation of 3C- and 4H-SiC using *in-situ* thermal cycling in nitrogen**
A. Constant [1, 2], N. Camara [1], P. Godignon [1], J. Camassel [2] and J.-M. Decams [3]
[1] CNM, Campus UAB, 08193 Bellaterra, Barcelona, Spain
[2] GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France
[3] Annealsys, Bat T2 PIT de la Pompignane, 34095 Montpellier cedex 1, France

9:45-10:00 **Ohmic and Schottky contacts on 3C-SiC epilayers grown by VLS and CVD**
Jens Eriksson [1, 2], Ming-Hung Weng [1], Fabrizio Roccaforte [1], Filippo Giannazzo [1], Raffaella Lo Nigro [1], Jean Lorenzzi [3], Sergey Reshanov [4], Giuseppe Baratta [5], Vito Raineri [1]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy
[2] Scuola Superiore - Università di Catania, Via San Nullo 5/i, 95123, Catania, Italy
[3] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France
[4] ACREO AB, Electrum 236, SE-16440 Kista, Sweden
[5] INAF- Astrophysical Observatory, University of Catania, Italy

10:00-10:15 **Low temperature photoluminescence investigations of 3C-SiC quasi-substrates grown on hexagonal 6H-SiC seeds**
G. Zoulis [1*], J. Lorenzzi [2], R. Vasiliauskas [3], N. Jegenyes [2], M. Beshkova [3], S. Juillaguet [1], H. Peyre [1], V. Souliere [2], M. Syväjärvi [3], G. Ferro [2], R. Yakimova [3], J. Camassel [1]
[1] GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France
[2] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France
[3] Department of Physics, Chemistry and Biology, Linköping University, Sweden

10:15-10:30 **Optical diagnostics of 3C/6H heterostructures grown by VLS+CVD techniques**
G. Manolis [1], J. Lorenzzi [2], N. Jegenyes [2], G. Ferro [2], K. Jarašiūnas [1]
[1] Institute of Materials Science and Applied Research, Vilnius University, Lithuania
[2] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France

10:30-10:45 **Structural and electrical characterization for 3C-SiC homoepitaxial layers**
M. Kato, Y. Iwata, Y. Matsushita, M. Ichimura
Nagoya Institute of Technology, Gokiso Showa Nagoya 466-8555, Japan

10:45-11:00 **Comparative study of oxides on n-type free standing 3C-SiC (001)**
R. Esteve [1,2], A. Schöner [1], S.A. Reshanov [1], C.-M. Zetterling [2], H. Nagasawa [3]
[1] ACREO AB, Electrum 236, SE-164 40 Kista, Sweden
[2] Dept. Information and Communication Technology, KTH, Electrum 229, Kista, Sweden
[3] SiC Development Center, Hoya Corporation, Japan

11:00-11:30 **Coffee Break**

Session 2 Sensors and MEMS

Chair: Jean Camassel *(GES, Université Montpellier 2, France)*

11:30-12:00 **Invited**
Sensors on 3C-SiC
Anita Spezl Lloyd
Linkoping University, Sweden

12:00-12:15
Polycrystalline 3C-SiC films deposited on 100 mm Si wafers for MEMS
A. Poggi [1], A. Schöner [2], A.Roncaglia [1], F. Bancarella [1], S. Milita [1], M. Bellei [3]
[1] CNR-IMM sezione di Bologna, Via Gobetti 101, 40129 Bologna, Italy
[2] ACREO AB-Electrum 236, Isafjordsgatan 22, SE-164 40 Kista, Sweden
[3] Medica s.r.l., Via degli Artigiani 6, 41036 Medolla- Modena , Italy

12:15-12:30
Stresses in SiC MEMS test structures
M. Bosi [1], G. Attolini [1], B.E. Watts [1], C. Frigeri [1], F. Rossi [1], A. Poggi [2], A. Roncaglia [2], F. Bancarella [2],V. Hortelano [3], O. Martinez [3]
[1] CNR-IMEM, Viale delle Scienze 37/a I-43100 Parma, Italy,
[2] CNR-IMM, Via Gobetti 10, I-40129, Bologna, Italy,
[3] Universidad de Valladolid, Fisica de la Materia Condensada-ETSII, 47011 VALLADOLID Spain

12:30-12:45
Novel high-*k* gas sensors for silicon carbide technology
Ming-Hung Weng [1,2], Rajat Mahapatra [1], Nick Wright [1], Alton Horsfall [1]
[1] School of Electrical, Electronic and Computer Engineering, Newcastle University, Newcastle upon Tyne, United Kingdom
[2] Present address: CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy

12:45-13:00
Towards high performant UV detectors in SiC
A. Sciuto [1], F. Roccaforte [1], M. Mazzillo [2], V. Raineri [1]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy
[2] ST Microelectronics, Stradale Primosole 50, 95121, Catania, Italy

13:00-15:00 **Lunch Break**

Session 3 3C-SiC on Si - I

Chair: Donat Josef As *(University of Pardebon, Germany)*

15:00-15:30 **Invited**
Elaboration and treatment of 3C-SiC heteroepilayers grown on silicon: from the material to GaN based applications
Marc Portail
CRHEA - CNRS, France

15:30-15:45
3C-SiC growth on off-axis Si substrates
A. Severino[1], M. Camarda[1], G. Condorelli[2], M. Mauceri[2], N. Piluso[1], R. Anzalone[1], B. Cafra[3], M.A. Di Stefano[3], A. La Magna[1], G. Abbondanza[2], F. La Via[1]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121 Catania, Italy
[2] Epitaxial Technology Center, 16ª Strada, Contrada Torre Allegra, 95030, Catania, Italy
[3] ST-Microelectronics, Stradale Primosole 50, 95121 Catania, Italy

15:45-16:00
TEM analysis of twins and interfacial defects in 3C-SiC grown on Si (111) by CVD
S. Roy [1], M. Portail [1], M. Zielinski [2], T. Chassagne [2],
[1] CNRS – CRHEA, Rue Bernard Grégory, 06560 Valbonne, France.
[2] NOVASIC, Savoie Technolac, 73375 Le Bourget du Lac Cedex, France

16:00-16:15
Epitaxial Growth of 3C-SiC on AlN/Si (100) via Methyltrichlorosilane-based Chemical Vapor Deposition
Wei-Cheng Lien [1], Kan Bun Cheng [2], Debbie Senesky [2], Carlo Carraro [1], Albert P. Pisano [2], Roya Maboudian [1]
[1] Department of Chemical Engineering, University of California, Berkeley, USA
[2] Department of Mechanical Engineering, University of California, Berkeley, USA

16:15-16:30
Growth and characterization of 3C-SiC grown using CBr_4 as a precursor
G.Attolini[1], M.Bosi[1], F.Rossi[1], B.E. Watts[1*], B. Pécz[2], L. Dobos[2] and G. Battistig[2]
[1] CNR-IMEM Institute Parco Area delle Scienze 37 A, 43010 Parma (Italy)
[2] Research Institute for Technical Physics and Materials Science, Hungarian Academy of Sciences, P.O. Box 49, H-1525 Budapest, Hungary

16:30-17:00 **Coffee Break**

Session 4 3C-SiC on Si - II

Chair: Roland Madar *(CNRS-LMGP, Grenoble, France)*

17:00-17:30 **Growth of cubic GaN and AlGaN/GaN on 3C-SiC**
Invited
Donat Josef As
University of Paderbon, Germany

17:30-17:45 **3C-SiC Epitaxial Layer grown on Si (001) and Si (001) 4° off-axis Substrates**
G. Wagner [1], J. Schwarzkopf [1], M. Schmidbauer [1], M. Luysberg [2], R. Fornari [1]
[1] Institut für Kristallzüchtung, Max-Born-Str. 2, D-12489 Berlin, Germany
[2] Forschungszentrum Jülich, Ernst-Ruska-Zentrum, D-52425 Jülich, Germany

17:45-18:00 **Numerical study of the evolution of substrate defects during the growth of epitaxial SiC films**
M. Camarda [1], A. La Magna [1], F. La Via [1]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy

18:00-18:15 **Comparison of 3C-SiC Films Grown on Si(001) and Si(111) via Hot-wall CVD**
C. Locke [1], R. Anzalone [2,3], A. Severino [2], C. Bongiorno [2], F. La Via [2], S. E. Saddow [1]
[1] Electrical Engineering Dept., University of South Florida, Tampa, FL,33620, USA
[2] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy
[3] University of Catania, Phys. Dept., via Santa Sofia 64, 95125, Catania, Italy

20:30 **Dinner**

Thursday May 7th 2009

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Session 5 Properties at nanoscale

Chair: Rositza Yakimova *(University of Linköping, Sweden)*

8:30-9:00 **Very large monolayer graphene ribbons grown on SiC**
Invited
Nicolas Camara
CNM-CSIC, Spain

9:00-9:15 **Investigation of graphene growth on 4H-SiC**
A. Castaing [1], O.J.Guy [1], M.Lodzinski [1], S.P.Wilks [1]
[1] School of Engineering, Swansea University, Singleton Park, Swansea SA2 8PP, UK

9:15-9:30 **Nanoscale current transport at graphene/SiC interface by scanning probe microscopy**
S. Sonde [1,2], F. Giannazzo [1], V. Raineri [1], R. Yakimova [3], J. Camassel [4]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy
[2] Scuola Superiore - Università di Catania, Via San Nullo 5/i, 95123, Catania, Italy
[3] Department of Physics, Chemistry and Biology, Linköping University, Sweden
[4] GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France

9:30-9:45 **Micro-Raman investigation of few graphene layers grown on 6H-SiC**
Jean Camassel [1,*], Jean-Roch Huntzinger, Antoine Tiberj[1], Mikael Syväjärvi[2], Rositza Yakimova[2], Filippo Giannazzo[3]
[1] GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France
[2] IFM, Linkoping University, Linkoping, Sweden
[3] CNR –IMM, Strada VIII, 5, 95121, Catania, Italy

9:45-10:15 **Silicon Carbide 3C/6H heterointerfaces**
Invited
Micheal G. Spencer.
Cornell University, USA

10:15-10:30 **Multiscale graphene quantum transport modeling and issues: the case of graphene epitaxially grown on SiC (0001)**
I. Deretzis [1,2], A. La Magna [2]
[1] Scuola Superiore - Università di Catania, Via San Nullo 5/i, 95123, Catania, Italy
2 CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy

10:30-11:00 **Coffee Break**

Session 6 Devices

Chair: Philippe Godignon *(CNM-CSIC, Spain)*

11:00-11:30 **SiC based materials for devices applications**
Invited Mike Capano
Purdue University, USA

11:30-12:00 **Technology and product trend of SiC power semiconductors at Infineon**
Invited Roland Rupp
Infineon Technologies, Germany

12:00-12:30 **Reduction of leakage current in MOSFETs fabricated on 3C-SiC substrate**
Invited Hiroyuki Nagasawa
SiC Development Center, Hoya Corporation, Japan

12:30-13:00 **Optical investigations techniques used for stacking faults characterization in SiC**
Invited Sandrine Juillaguet
Groupe d'Etude des Semiconducteurs, CNRS and Université Montpellier 2, France

13:00-15:00 **Lunch Break**

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Session 7 Properties and Characterization

Chair: Efstathios Polychroniadis (*Aristotle University of Thessaloniki, Greece)*

15:00-15:30 **Development of methods for dislocation characterization in SiC materials and devices**
M. Dudley , N. Zhang, Y. Chen
Stonybrook University, USA

15:30-16:00 **Optical characterization of wide bandgap semiconductors at excitation conditions approaching power device operation**
K.Jarašiūnas, T.Malinauskas, R.Aleksiejūnas, S.Nargelas, P. Ščajev, G.Manolis, V.Gudelis
Institute of Materials Science and Applied Research, Vilnius University, Lithuania

16:00-16:30 **Application of SIMS and SNMS to mixed matrix semiconductor materials.**
Graham Cooke
Hiden Analytical LTD, United Kingdom

16:30-17:00 **Physical analysis of Si-on-SiC by direct wafer bonding**
M. R. Jennings [1], A. Pérez-Tomás [1], O. J. Guy [2], M. Lodzinski [2], P. Gammon [1], S. Burrows [1], J. A Covington [1], P. A. Mawby [1]
[1] School of Engineering and Physics Dept., University of Warwick, Coventry, UK
[2] School of Engineering, University of Wales, Swansea, UK

17:00-17:30 **Coffee Break**

17:30-19:00

Joint poster session HeteroSiC – WASMPE

P1 **Heteroepitaxy of 3C-SiC on different on-axis oriented Silicon substrates**
R. Anzalone [1,2], A. Severino [1], G. D'Arrigo [1], C. Buongiorno [1], G. Abbondanza [3], G. Foti [1], S. Saddow [4] , F. La Via [1]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy
[2] University of Catania, Phys. Dept., via Santa Sofia 64, 95125, Catania, Italy
[3] Epitaxial Technology Center, 16° Strada,, Con.da Torre Allegra, 95030, Catania, Italy
[4] Dept. of Electrical Engineering, University of South Florida, Tampa, Florida, USA

P2 **Growth and characterization of β−SiC and SiO2/β−SiC core-shell nanowires**
G.Attolini, F.Rossi, M.Bosi, B.E.Watts, F.Fabbri, G.Salviati
CNR-IMEM Institute, Parco Area delle Scienze 37A, 43010 Parma (Italy)

P3 **Influence of defect density to the Schottky barrier height on a 3C/4H-SiC heterostructure**
Ming-Hung Weng [1], Jens Eriksson [1, 2], Fabrizio Roccaforte [1], Filippo Giannazzo [1], Salvatore Di Franco [1], Corrado Bongiorno [1], Stefano Leone [3], Vito Raineri [1]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy
[2] Scuola Superiore - Università di Catania, Via San Nullo 5/i, 95123, Catania, Italy
[3] Department of Physics, Chemistry and Biology, Linköping University, Sweden

P4 **Electrical transport properties of catalyst-free grown 3C-SiC nanowires**
K. Rogdakis [1,2], E. Bano [1], L. Montes [1], M. Bechelany [3], D. Cornu [4], K. Zekentes [2]
[1] IMEP-LAHC/INPG , MINATEC, 3, parvis Louis Neel-BP 257, Grenoble Cedex 01, France
[2] MRG-IESL/ FORTH, Vassilika Vouton, Greece
[3] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France
[4] IEM-MAAS/ENSCM, 8 rue de l'Ecole Normale, Montpellier Cedex 05, France

P5 **On the structural defects and the polytype stabilization in LPE grown 6H-SiC layers**
I. G. Galben-Sandulache [1], F. Mercier [1], M. Marinova [2], D. Chaussende [1], E. K. Polychroniadis [2]
[1] Laboratoire des Matériaux et du Génie Physique CNRS UMR 5628, Grenoble INPMinatec, BP 257, 38016 Grenoble Cedex 01, France
[2] Departement of Physics, Aristotle University of Thessaloniki, Greece

P6 **The effect of different substrate preparations on growth of cubic silicon carbide**
R. Vasiliauskas[1], M. Syväjärvi[1], M. Beshkova [1], J. C. Lorenzzi [2], G. Ferro [2], R.Yakimova [1]
[1] Department of Physics, Chemistry and Biology, Linkoping University, Sweden
[2] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France

P7 **Evaluation of Ni and Pt Schottky barrier height in a 3C-SiC/Si vertical structure**
A.E. Bazin [1,2], J.F. Michaud [1], T. Chassagne [3], M. Zielinski [3], M. Portail [4], E. Collard [2], D. Alquier [1]
[1] Université François Rabelais, Tours, L.M.P, 37071 Tours Cedex 2, France
[2] ST Microelectronics, 37071 Tours Cedex 2, France
[3] NOVASIC, Savoie Technolac, 73375 Le Bourget du Lac Cedex, France
[4] Centre de Recherche sur l'Hetero-Epitaxie et ses Applications CNRS, Valbonne, France

P8 **Effect of growth parameters on the surface morphology of 3C-SiC homoepitaxial layers grown by chemical vapor deposition**
N. Jegenyes[1*], J. Lorenzzi[1], G. Zoulis[2], V. Soulière[1], J. Dazord[1], S. Juillaguet[2], G. Ferro[1]
[1] LMI, UMR-CNRS 5615, UCB-Lyon1, 69622 Villeurbanne, France
[2] GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France

P9 **On the structure of different long-period SiC polytypes by means of electron diffraction and high resolution transmission electron microscopy**
M. Marinova [1], E.K.Polychroniadis [1]
[1] Department of Physics, Aristotle University of Thessaloniki, Greece

P10 **Observation of 3C zigzag faults in low-doped 4H-SiC epitaxial layers**
T. Robert[1], M. Marinova[2], S. Juillaguet[1], A. Henry[3], E.K. Polychroniadis[2], J. Camassel [1,*]
[1] GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France
[2] Department of Physics, Aristotle University of Thessaloniki, Greece
[3] IFM departement, Institute of Technology, Linköping University

P11 **"In situ" Low Temperature Photoluminescence in ion irradiated 4H-SiC**
G. Litrico [1], M. Zimbone [1], L. Calcagno [1], P. Musumeci [1], G. A. Baratta [2], G. Foti [1]
[1] Department of Physics and Astronomy, Catania University, 95123. Catania, Italy
[2] INAF- Astrophysical Observatory, Catania University, 95123 Catania, Italy

P12 **Electrical and optical properties of *p*-type ZnO films grown on sapphire**
J. W. Sun [1,2], Y. M. Lu [1], Y. C. Liu [1], D. Z. Shen [1]
[1] Key Laboratory of Excited State Processes, Changchun Institute of Optics, Fine Mechanics and Physics, Chinese Academy of Science, 130033 Changchun, P. R. China
[2] Present address : GES, UMR-CNRS 5650, Université Montpellier 2, 34095 Montpellier cedex 5, France

P13 **Two-dimensional electron gas isolation in AlGaN/GaN devices**
F. Roccaforte [1], F. Iucolano [1], F. Giannazzo [1], S. Di Franco [1], G. Abagnale [2], V. Puglisi [2], V. Raineri [1]
[1] CNR-IMM, Strada VIII, n.5, Zona Industriale, 95121 Catania – Italy
[2] ST Microelectronics, Stradale Primosole 50, 95121 Catania - Italy

P14 **Electron mobility in GaN solving the Boltzmann equation**
C. Miccoli [1,2], A. Majorana [3]
[1] Dipartimento di Fisica e Astronomia, Università di Catania, Italy
[2] ST Microelectronics, Stradale Primosole 50, 95121 Catania, Italy
[3] Dipartimento di Matematica e Informatica, Università di Catania, Italy

P15 **Defects and electrical activation of Al ion-implanted 4H-SiC for power MOSFETs**
Ming-Hung Weng [1], Fabrizio Roccaforte [1], Filippo Giannazzo [1], Raffaella Lo Nigro [1], Corrado Buongiorno [1], Salvatore Di Franco [1], Edoardo Zanetti [2], Alfonso Ruggiero [2], Mario Saggio [2], Vito Raineri [1]
[1] CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy
[2] ST Microelectronics, Stradale Primosole 50, 95121, Catania, Italy

P16 **Nanoscale electrical characterization of wide-bandgap semiconductors materials and devices**

F. Giannazzo, F. Roccaforte, F. Iucolano, Ming-Hung Weng, S. Di Franco, V. Raineri
CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy

P17 **Sub-micrometer dielectric properties in advanced dielectrics for Rf technology**
Patrick Fiorenza, Raffaella Lo Nigro, Vito Raineri
CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy

P18 **Al^+ implanted 4H-SiC P-i-N diodes: SIMS, C-V and DLTS characterizations**
R. Nipoti [1], F. Fabbri [2], F. Moscatelli [1], A. Poggi [1], A. Cavallini [3], A. Carnera [4]
[1] *CNR-IMM, via Gobetti 101, 40129 Bologna, Italy*
[2] *IMEM-CNR, viale Usberti 37/A, 43100 Parma, Italy*
[3] *Phods Lab, Department of Physics, University of Bologna, and CNISM, Bologna, Italy*
[4] *Department of Physics, University of Padova, via Marzolo 8, 35131 Padova, Italy*

21:00 **Social Dinner**

Friday May 8th 2009

WASMPE 2009

Session 8 Power Devices

Chair: Adolf Schöner *(ACREO AB, Sweden)*

8:30-9:00 **SiC technology for power devices fabrication in a standard industrial environment**
M. Saggio[1], F. Giannazzo[2], F. Roccaforte[2], A. Ruggiero[1], E. Zanetti[1],
[1] *STMicrolectronics IMS R&D, Stradale Primosole 50, 95121 Catania, Italy*
[2] *CNR IMM, Strada VIII n.5, Zona Industriale, 95121 Catania, Italy*

9:00-9:30 **A step toward fully integrated monolithic driver for 1.2kV-3.5kV SiC-BJT high temperature applications**
D. Tournier [1], P. Bevilacqua [1], P. Brosselard [1], D. Planson [1], B. Allard [1]
[1]*Ampere (UMR CNRS 5005), INSA de Lyon, 69621 Villeurbanne cedex, France*

9:30-10:00 **Towards high power Schottky diodes in GaN: main challenges**
F. Iucolano[1*], F. Roccaforte[1], F. Giannazzo[1], S. Di Franco[1], V. Puglisi[2], V. Raineri[1]
[1] *CNR-IMM, Strada VIII n.5, Zona Industriale, 95121 Catania - Italy*
[2] *ST-Microelectronics, Stradale Primosole 50, 95121 Catania - Italy*

10:00-10:30 **Power devices in GaN on Si**
Marianne Germain
IMEC, Belgium

10:30-11:00 **Planar Schottky diodes made on gallium nitride (GaN) grown on sapphire: Impact of the process parameters.**
O. Menard [1,2], F. Cayrel [1], E. Collard [2], D. Alquier [1]
[1] *Université François Rabelais, Tours, L.M.P, 37071 Tours Cedex 2, France*
[2] *ST Microelectronics, 37071 Tours Cedex 2, France*

11:00-11:30 **Coffee Break**

Session 9 Material and Devices

Chair: Owen Guy (*University of Wales, Swansea, United Kingdom)*

11:30-12:00 **The heterojunction properties of a novel Ge/SiC semiconductor structure**
P. M. Gammon [1], A. Pérez-Tomás [2], M. R. Jennings [1], G. J. Roberts [1], V. A. Shah [3], J. A. Covington [1], P. A. Mawby [1]
[1] *School of Engineering, University of Warwick, Coventry CV4 7AL, United Kingdom*
[2] *Centre Nacional de Microelectrónica, Campus UAB, 08193 Barcelona, Spain*
[3] *Department of Physics, University of Warwick, Coventry CV4 7AL, United Kingdom*

12:00-12:30 **Recent progress in diamond electronics**
D.Doneddu [1,2], O.J.Guy [2], A.Castaing [2], M.Lodzinski [2]
[1] *Global Academy, University of Wales, Kings Road, Swansea SA1 8PH United Kingdom*
[2] *School of Engieering, Swansea University, Swansea SA2 8PP United Kingdom*

12:30-13:00 **Metal contacts to boron-doped diamond**
M. Lodzinski [1], O.J. Guy [1], A. Castaing [1], S. Batcup [1], S. Wilks [1], D. Doneddu [1], P. Igic [1], R.

Balmer [2], C. Wort, R. Lang [2]
[1] School of Engieering, Swansea University, Swansea SA2 8PP United Kingdom
[2] Diamond Microwave Devices Ltd, Leeds Innovation Centre,Leeds, Yorkshire, UK

13:00-15:00 **Lunch Break**

Session 10 Power RF devices - I

Chair: Roberta Nipoti *(CNR-IMM, Bologna, Italy)*

15:00-15:30 **GaN/AlGaN HEMTs for RF applications**
E. Limiti, W. Ciccognani, M. Ferrari
Università di Roma "Tor Vergata", Italy

15:30-16:00 **Design, process, and performance of all-epitaxial double-gate trench SiC JFETs**
Rajesh Kumar Malhan[1*], Yuuichi Takeuchi[1], Naohiro Sugiyama, Adolf Schöner [2]
[1] DENSO Corporation, Research Laboratories, Nisshin, Aichi 470-0111, Japan
[2]ACREO AB, Electrum 236, Isafjordsgatan 22, SE-164 40 Kista, Sweden

16:00-16:30 **Prospects and Challenges for GaN HFETs in Wireless Basestation Applications**
Peter Asbeck
University of California, San Diego - USA

16:30-17:00 **Development of Semi Insulating SiC for RF devices**
Andy Souzis
II-VI, USA

17:00-17:30 **Coffee Break**

Session 11 Power RF devices - II

Chair: Peter Asbeck *(University of California, San Diego, USA)*

17:30-18:00 **GaN/AlGaN HEMTs for RADAR applications**
Claudio Lanzieri
Selex-SI, Italy

18:00-18:30 **Three terminal Breakdown evaluation in GaN-HEMT Devices**
Augusto Tazzoli, Enrico Zanoni, Gaudenzio Meneghesso
DEI, University of Padova, Via Gradenigo 6/B, 35131, Padova, Italy

18:30-19:00 **The influence of AlN/AlGaN/GaN transition layers on breakdown simulation of an AlGaN/GaN HEMT**
C. Miccoli [1,2], G. Abagnale [1], S. Reina [1], V. Puglisi [1], V. Cinnera Martino [1], S. Rinaudo [1]
[1] ST Microelectronics, Stradale Primosole 50, 95121 Catania, Italy
[2] Dipartimento di Fisica e Astronomia, Università di Catania, 95123, Catania, Italy

19:00 **Conclusions**

Growth and characterization of low doped 3C-SiC layers deposited by the VLS technique

J. Lorenzzi[1*], G. Zoulis[2], O. Kim-Hak[1], S. Juillaguet[2], G. Ferro[1] and J. Camassel[2].
[1]*Laboratoire des Multimateriaux et Interfaces, UMR-CNRS 5615, UCB-Lyon1, 43 Bd du 11 nov. 1918, 69622 Villeurbanne, France*
[2]*Groupe d'Etude des Semiconducteurs, CNRS and Université Montpellier 2, cc 074-GES, 34095 Montpellier cedex 5, France*
[*] Corresponding author: jean.lorenzzi@univ-lyon1.fr

Most present SiC power electronic devices are made from the 4H-SiC polytype. The 3C-SiC polytype is also considered, mainly because it could be advantageous to solve some of the specific problems encountered in MOS (Metal-Oxide-Semiconductor) technology. Controlling then the purity of the epitaxial layers used to build the n-type and p-type channels is a prerequisite.

Since there is no large diameter 3C-SiC substrate commercially available, high quality 3C-SiC heteroepitaxial layers grown on α-SiC(0001) substrates must be used. In this case, to convert the 6H-SiC seed into a 3C-SiC layer, the growth technique already known as VLS (Vapour-Liquid-Solid) mechanism is a well established method [1]. Basically, one feeds a Si-Ge melt with propane gas to nucleate and grow 3C-SiC material. Unfortunately the as-grown layers present usually a high level of residual (n-type) doping, with typical values ranging from ~ 5.10^{17} to 5.10^{18} cm^{-3}. This depends only on the deposition conditions. Reduction to a lower value is needed.

In this work, we report the results of a systematic investigation done to modify the usual growth procedure. We performed careful and prolonged out-gasing steps at room temperature and 850°C. Care was taken not to exceed the Ge melting point and, in addition, pieces of Zr-Ti alloys were placed beside the crucible to act as N getter. The out-gasing conditions were chosen in such a way that it did not affect the layer crystalline quality, nor degrade the usual surface morphology.

In this way, our best sample was a monodomain, (111)-oriented, 3C-SiC layer grown with a $Si_{25}Ge_{75}$ melt fed by 5 sccm of C_3H_8 using the two-step procedure (1450-1200°C) described in [2]. The resulting growth rate was 2 μm/h. The residual doping level was investigated by μ-Raman spectroscopy and low temperature photoluminescence (LTPL) spectroscopy. From the deconvolution of the LO peak of the Raman spectra, the n type doping level could be systematically estimated below 10^{17} cm^{-3}. This was confirmed by LTPL measurements.

At liquid helium temperature all spectra displayed well-resolved N-bound exciton lines, typical of low doped material. From the FHWM of the TA mode and using a calibration curve extracted from the work of Ref [3], the n type doping was estimated to be ~4.10^{16} cm^{-3}. A weak signal was attributed to Al-N donor-acceptor pairs (DAP) but the intensity was very low. From the experimental spectra, the estimated Al concentration was estimated around 5.10^{15} cm^{-3}, meaning that the level of compensation did not exceed 10%.

This work has been supported by EU in the framework of the MANSiC project (Grant No. MRTN-CT-2006-035735).

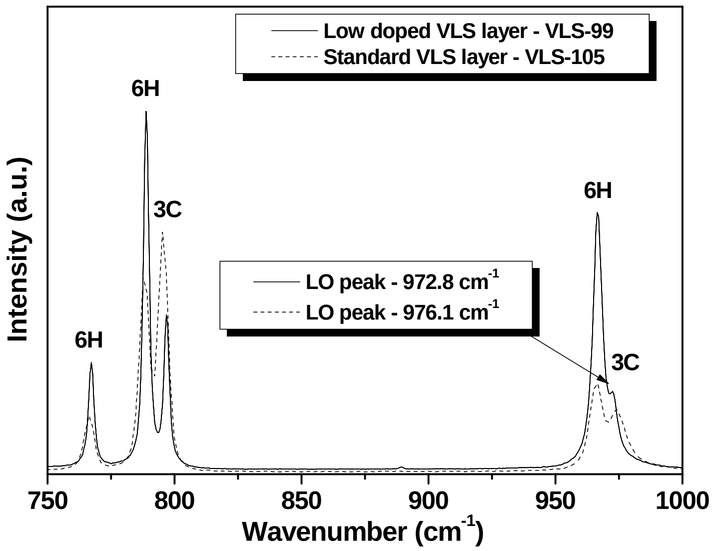


Fig. 1: Raman spectra of 3C-SiC layers grown by VLS using standard (red) and optimized (black) procedures

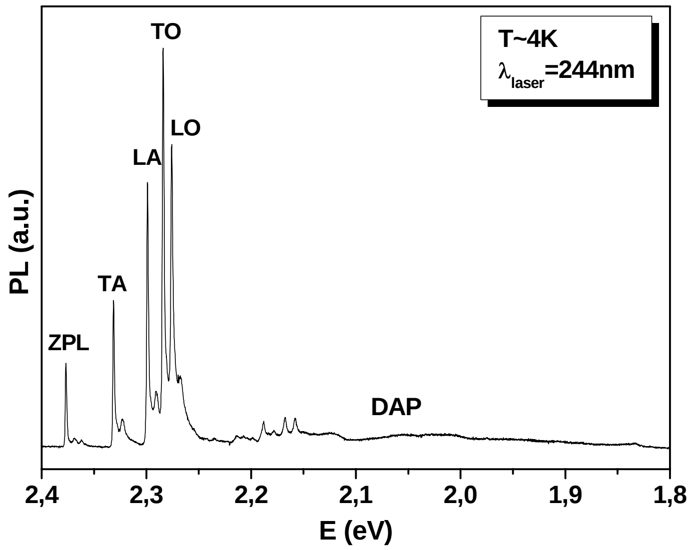


Fig. 2: LTPL spectrum collected at 4K on a high purity 3C-SiC VLS layer.

References

[1] M. Soueidan et al., Crystal Growth & Design **6**, No. 11, 2598 (2006)
[2] M Soueidan et al, Crystal Growth & Design **8** N°3, 1044 (2008)
[3] J. Camassel et al., Chem. Vap. Deposition 1**2**, 549 (2006)

TEM study of 3C-SiC layers grown by sublimation epitaxy on 6H-SiC substrates

M. Marinova[1,*], M. Beshkova[2], A. Mantzari[1], M.Syväjärvi[2], R. Yakimova[2], E.K.Polychroniadis[1]
[1]*Department of Physics, Aristotle University of Thessaloniki, GR54124 Thessaloniki, Greece*
[2]*Department of Physics, Chemistry and Biology, Linköping University, SE-58183 Linköping, Sweden*
[*] Corresponding author: marinova@physics.auth.gr

Among the many SiC polytypes, the cubic one has the lowest band gap energy and several advantages over the most commonly used hexagonal polytypes: more isotropic properties, higher mobility, and a lower oxide interface trap density. However, main problems are the polytype stabilisation and the appearance of in-grown defects. Most common issues related to defects formation are the occurrence of coherent and incoherent double position boundaries and the formation of stacking faults (SFs). Thus it is of great significance to investigate the influence of different growth parameters on the polytype stabilisation and the type and density of defects appearing in the grown layers.

In the present work the structural quality of 3C-SiC grown by sublimation epitaxy is studied by Transmission Electron Microscopy (TEM). The layers were grown on on-axis, Si-face, 6H-SiC substrates at source temperature 2000°C and different temperature gradients, ranging from 5 to 8 ºC/mm. The dependence of the 3C - 6H polytype transition, 3C stabilisation and SF density on the different temperature gradients is discussed. The highest temperature gradient favours formation of 3C-SiC layers free of 6H-SiC inclusions. Nevertheless the formation of complicated multiple twin structures nucleated at the interface with the 6H-SiC substrates, where the double positioning appears, both in the (111) and $\{\bar{1}11\}$ planes, is observed systematically. This is presented in Fig.1 where a conventional TEM image from the layer grown at the highest temperature gradient is shown. The corresponding diffraction pattern (DP) allows the identification of the relation between the different DPBs. The double positioning for the twin couples T_1/T_2, and T_3/T_4 appears along the $\{\bar{1}11\}$ planes. The case of T_2/T_3 is more complicated. In this case the twin is incoherent as the contact plane does not coincide with the twin plane, something that is clearly seen in the higher resolution image (Fig.2). The contact plane is even inclined to the observation plane (i.e. the $(0\bar{1}1)$ plane of the 3C-SiC), something which is easily understood from the width of the contact plane in the presented conventional TEM micrograph (Fig.1).

By lowering the temperature gradient the amount of 6H-SiC inclusions increases, but the nucleated 3C-SiC exhibits better crystalline quality with low SF density as shown in Fig. 3. At the lowest temperature gradient the 3C-6H-SiC boundary appears to facets parallel to the particular planes, (0001) and $(1\bar{1}0n)$, n=0,2,4, following a zig-zag propagation as shown in Fig. 4. It is noteworthy that the epitaxial relationship changes to $(111)_{3C}||(1\bar{1}02)_{6H}$. On the contrary the 3C-6H-SiC transition at higher temperature gradients does not show specific crystallographic orientation. The finding in this work resolves the relationship between nucleation and competing mechanisms to the crystal quality and polytype formation, which will critically determine successful growth of 3C-SiC substrates.

The work was performed within the MANSiC project (MRTN-CT-2006-035735)

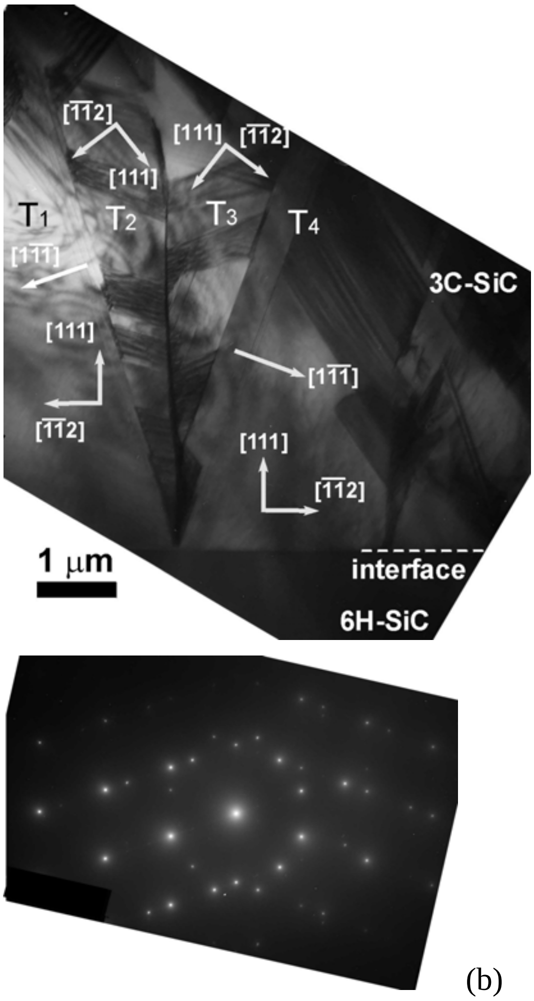


Fig. 1. (a) A conventional TEM image and (b) the corresponding DP from the layer grown at the highest temperature gradient, where complicated twin complexes starting form the interface with the 6H-SiC substrate are formed.

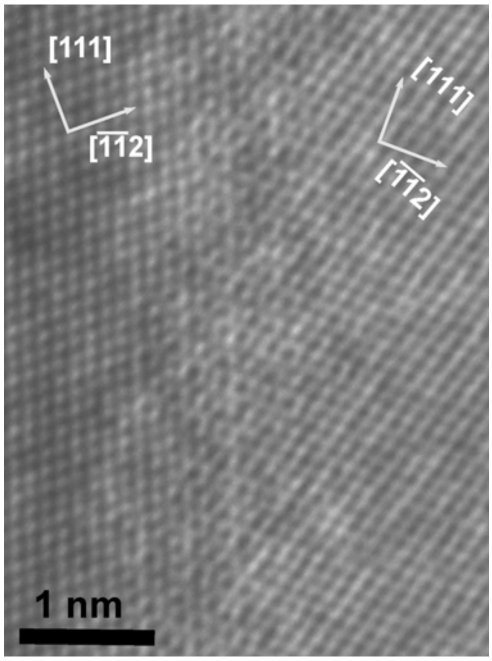


Fig. 2. HRTEM image of T_2/T_3 DPB.

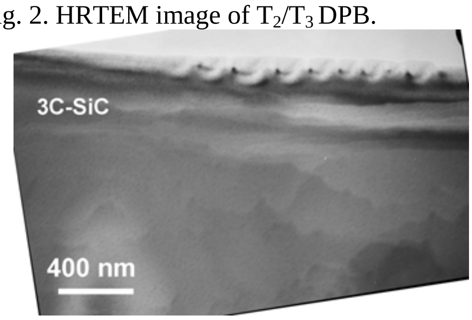


Fig. 3. A TEM image from the layer grown at temperature gradient 6 ºC/mm. The 3C-SiC formed exhibits strongly reduced defect density.

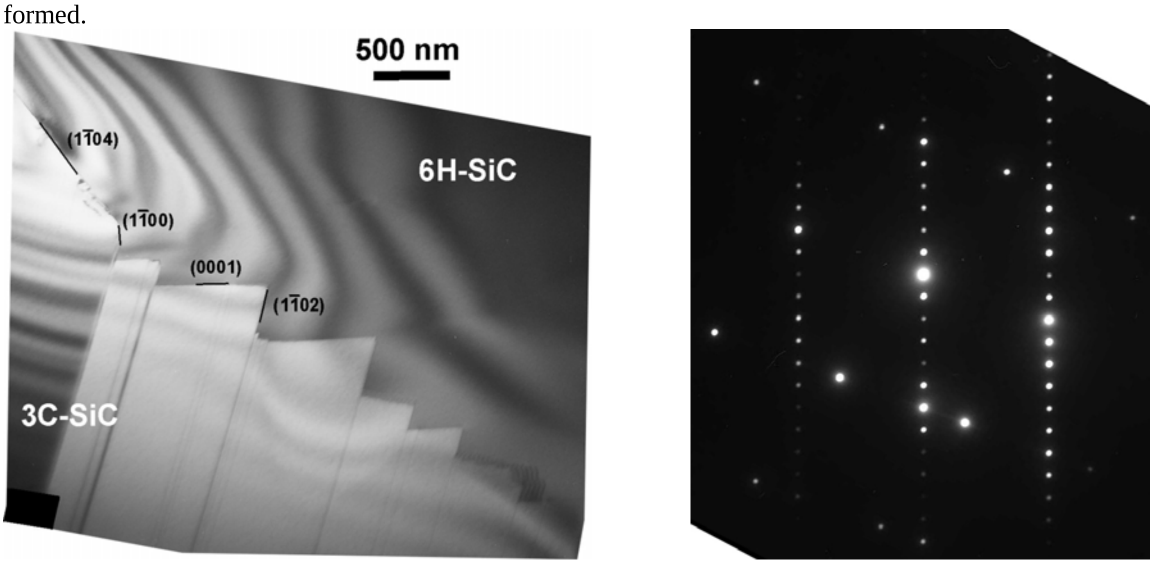


Fig. 4. A TEM image and the corresponding DP from the layer grown at the lowest temperature gradient 5 ºC/mm, showing characteristic 3C-6H-SiC interface.

Sublimation epitaxy of 3C-SiC-growth and characterization

M. Beshkova[1], J. Lorenzzi[2], N. Jegenyes[2], R. Vasiliaskas[1], J. Birch[1], M.Syväjärvi[1], G. Ferro[2], R. Yakimova[1]

[1]*Department of Physics, Chemisty and Biology, Linköping University, SE-58183 Linköping, Sweden*

[2]*Laboratoire des Multimateriaux et Interfaces, UMR-CNRS 5615, UCB-Lyon1, 43 Bd du 11 nov. 1918, 69622 Villeurbanne, France*

* Corresponding author: milbe@ifm.liu.se

Silicon carbide is considered to be a strategic semiconductor for high-temperature, high-power and high-frequency device applications. The most common polytypes of SiC are 4H, 6H and 3C, the later being the only cubic phase with isotropic physical properties. The 3C-SiC polytype has the highest electron mobility, which is an important parameter of a material to be used in device fabrication for certain applications [1].

3C-SiC substrates are still not manufactured industrially, and therefore, 3C-SiC layers are most frequently grown on silicon substrates. However due to the 20% lattice misfit between Si and 3C-SiC the structural quality is poor.

The present work deals with morphological and structural investigations of 3C-SiC layers grown by sublimation epitaxy at source temperature 2000°C under vacuum condition ($<10^{-5}$ mbar) and temperature gradient of 7°C/mm.

The growth was performed in a sandwich system described elsewhere [2].

Four types of substrates were used: Type I and II were on axis 6H-SiC (0001) with and without additional polishing, respectively. Type III was on axis 6H-SiC with a seed layer of 3C-SiC grown by vapor-liquid-solid (VLS) mechanism while Type IV was prepared with a seed layer grown sequentlialy by VLS and chemical vapor deposition (CVD). The optical microscopy in transmission mode revealed domain character for the layers grown on bare 6H-SiC substrates and continuous character for the layers grown on 6H-SiC with 3C-SiC seed layers Fig.1. The layers grown on Type III and IV substrates exhibit specific pit-like defects.

Table 1 depicts the layer thickness, percentage of 6H-SiC inclusion (estimated from an area of 4 mm^2) and full width at half maximum (FWHM) of ω-curves of 3C-SiC (111) reflection from high resolution X-ray diffraction (HRXRD) measurements.

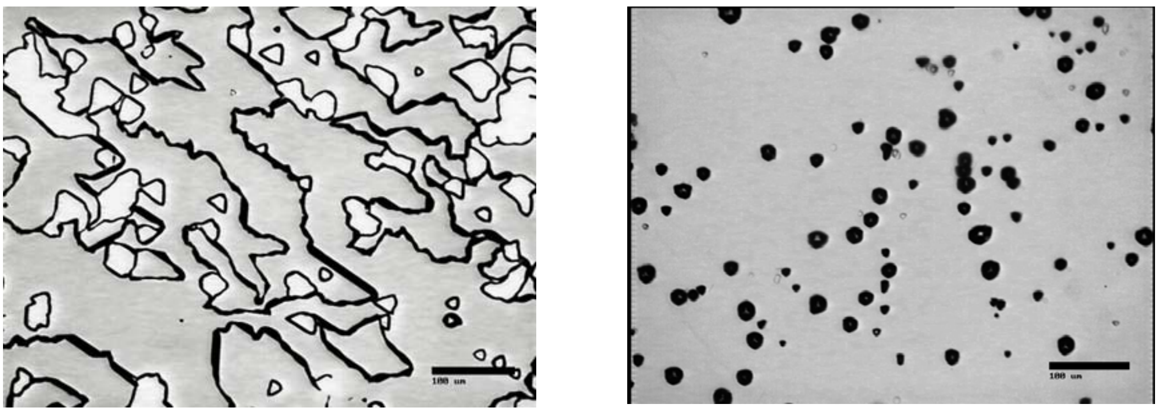
FWHM of 3C-SiC (111) reflection is smaller for samples grown on substrate with seed layer which suggests better crystalline quality.

Atom force microscopy (AFM) images for all samples exhibit single-bilayer (0.25 nm) height steps which is characteristic of 3C-SiC [3] , and terraces with average width 660 nm and 390 nm for 3C-SiC layer grown on substrate Type I, II and Type III, IV respectively Fig. 2.

The work was performed within the MANSIC project (MRTN-CT-2006-035735)

Table1. Layer thickness, percentage of 6H-SiC inclusion and FWHM (111) of ω-curves for 3C-SiC grown on different type of substrates.

Substrate type	Type I	Type II	Type III	Type IV
Layer thickness [μm]	20	29	24	18
6H inclusion [%]	2	0.2	0	0
FWHM (111) [arcsec]	179	302	144	83



a) b)

Fig.1: Optical microscope image in transmission mode taken from samples grown on substrate Type I (a) and IV (b), respectively. The scale bar is 100 μm. The colors on the picture are not original because of the grey scale, the grey corespond to 3C-SiC and white to 6H-SiC inclusion.

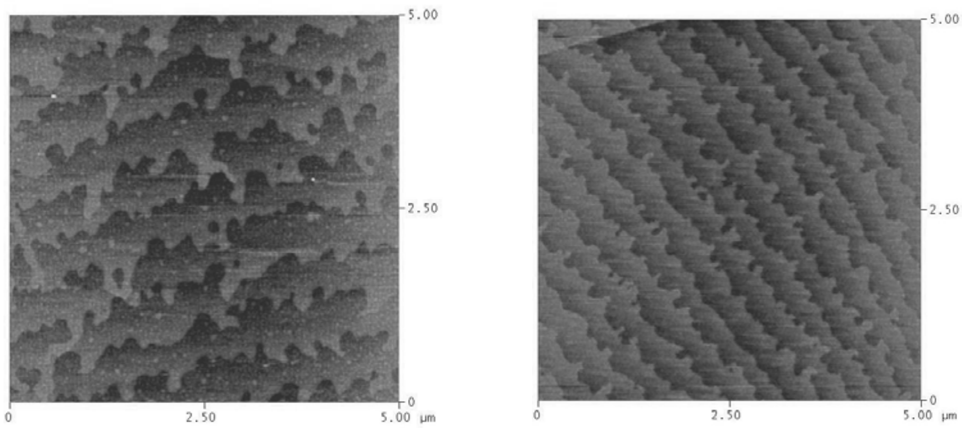


Fig. 2: AFM image from 3C-SiC layers grown on substrate Type I (a) and IV (b), respectively, showing different terrace width.

References

[1] K Lee, G Pensl, M Soueidan, G Ferro, Y Monteil, Jpn. J. Appl. Phys. **45**, 6823 (2006)
[2] M Beshkova, M Syväjärvi, R Vasiliauskas, J Birch and R Yakimova, Mat Sci Forum **615-617,** 181 (2009)
[3] P Neudeck, A Trunek, D Spry, J Powell, H Du, M Skowronski, X Huang and M Dudley, Chem.Vap. Deposition **12**, 531 (2006)

Rapid thermal oxidation of 3C- and 4H-SiC using *in-situ* thermal cycling in nitrogen

A. Constant[1, 2*], N. Camara[1], P. Godignon[1], J. Camassel[2] and J.-M. Decams[3]
[1]*CNM, Campus UAB, 08193 Bellaterra, Barcelona, Spain*
[2]*GES, UMR-CNRS 5650 and Université Montpellier 2,*
34095 Montpellier cedex 5, France
[3]*Annealsys, Bat T2 PIT de la Pompignane, 34095 Montpellier cedex 1, France*
[*] Corresponding author: aurore.constant@imb-cnm.csic.es

Silicon carbide (SiC) is a most promising material for high-power, high-temperature electronic device applications. A decisive advantage over the other wide-band gap semiconductors is the possibility to form an insulating SiO_2 layer by thermal oxidation. This provides a great opportunity to develop a specific Metal Oxide Semiconductor (MOS) technology to complement Si. Unfortunately the poor quality of the SiC/SiO_2 interface, and the low oxide reliability, are critical factors that up to now limited the development of the SiC industry. Basically, any non complete elimination of the carbon species, oxidation of the excess Si ones and/or passivation of Si- and C- dangling bonds at the interface produce electrically active complexes acting as deleterious defects for the SiC/SiO_2 interface (and related oxide quality).
A most effective technique for interface traps passivation and carbon removal is the use of nitridation, which includes either direct oxide growth or post oxidation annealing in nitrogen (N) or a N-containing mixture. A main drawback is that such nitridation techniques applied to SiC thermal oxidation require a huge thermal budget in conventional furnaces, of the order of ~1100ºC for several hours [1-2]. To reduce this thermal budget, oxide formation in a N-contained gas by Rapid Thermal Processing (RTP) seems a promising alternative. Thanks to the existence of highly energetic photons, a much lower thermal budget is needed for growing the same oxide thickness. In this work we show that RTP in a N-containing gas mixture is not only a fast technique to grow SiO_2, it improves also the quality of the oxide on 3C and 4H-SiC substrates.
Oxidation experiments were done on (001) n-type 3H-SiC/Si and 4H-SiC samples. The epitaxial layers had a doping concentration of ~ 5×10^{17} cm^{-3} and 5×10^{15} cm^{-3}, respectively (Nitrogen doping). Before oxidation, they were prepared by HF and RCA cleaning. All samples were loaded and unloaded at room temperature in N_2 in a RTP furnace (AsOne 100 from Annealsys) schematised in Figure 1. Thermal oxidation was carried out in an O_2 ambient at 1050 °C during 180 s under atmospheric pressure. To study the effect of in-situ nitridation, the process gas was either O_2 or O_2 diluted with N_2 ($[O_2]$ = [100%; 50%; 20%]). Then, a rapid post oxidation annealing (RTA) step was done under N_2 above oxidation temperature and, finally, the sample was cooled down gradually using a ramp-down rate of -83 °C/min. This thermal cycle is shown in Figure 2. The electrical properties of the SiO_2/SiC structures were then evaluated using a mercury probe. To this end, C-V, G-V and I-V measurements were done at room temperature.
A first result is that the oxide thickness is *not* proportional to the O_2 partial pressure in the gas mixture. Using for O_2 partial pressures of 1 / 0.5 and 0.2 atm, we find for the 3C-SiC oxide thicknesses ~ 18 nm, 19 nm and 8 nm, respectively, while for 4H-SiC we find 16 nm, 15 nm nm and 10 nm, respectively. This gives oxide grown rates that vary from ~ 5 nm per min in pure O_2 to ~ 3 nm per min for a 80% N-mixture in, both, 3C and 4H-SiC which are to be compared with the much lower values found in a classical furnace to obtain the same final oxide thickness (typically 0.16 nm per min [3] and 0.06 nm per min [4] at 1050 ºC for 3C and 4H-SiC, respectively). This is about 35 and 80 times faster for 3C- and 4H-SiC, respectively.
From the C-V curves collected at 1 MHz, we found also that the oxides grown in 80% N_2 exhibited a large improvement in oxide quality and SiO_2/SiC interfaces compared to the one

grown in 50% N_2 or pure O_2. This is shown in Figure 3. We find a reduction in, both, the hysteresis and the flat-band voltage. This suggests that the best oxidation process occurs when the kinetics of carbon removal or passivation (nitride effect) keep pace with the carbon generation (oxidation) process. This gives a slower growth rate, but not so much. Hence, we deduce that the accumulation of carbon species in the oxide bulk reduces as the oxidation and nitridation passivation processes are in equilibrium.
Thanks to this benefit, short processing times can be achieved, reducing then the thermal budget, thermal stress and total processing time of SiC wafers.
This work has been supported by EU in the framework of the MANSiC project (Grant No. MRTN-CT-2006-035735).

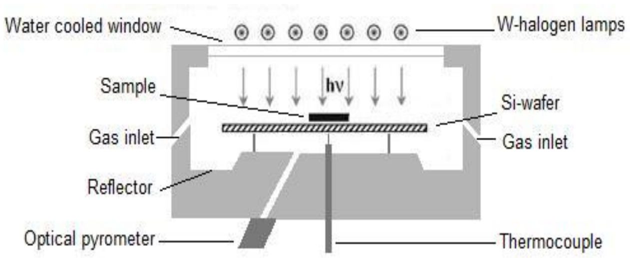


Fig.1: Schematics of the AsOne RTP furnace used in this work.

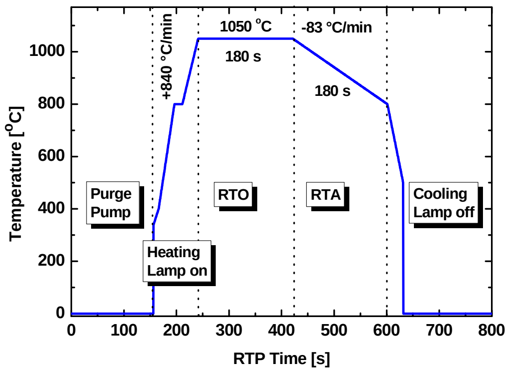


Fig.2: Schematics of the *in-situ* RTP sequence, including Rapid Thermal Oxidation (RTO) and Rapid Thermal Anneal (RTA) steps.

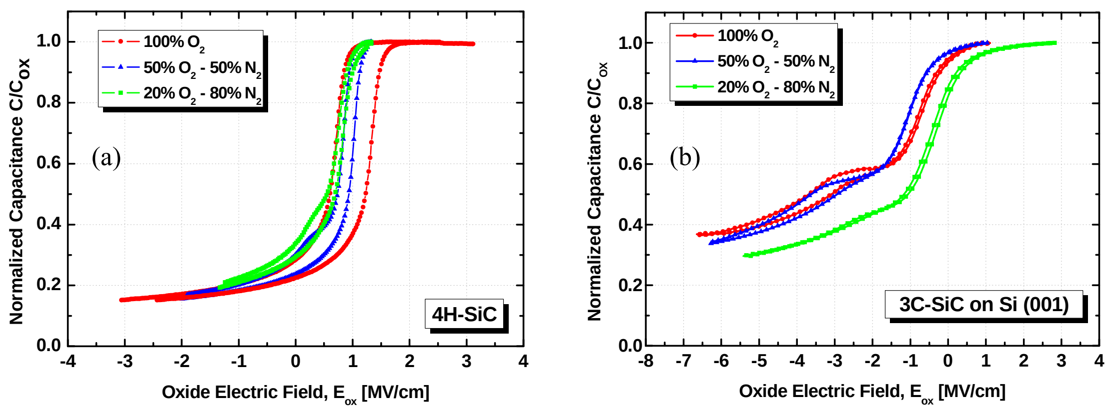


Fig.3: Comparison of the high frequency (ω = 1 MHz) C-V characteristics collected for oxides grown on 4H-SiC (a) and 3C-SiC (b) by rapid thermal oxidation during 180 s for different O_2/N_2 mixtures (1050 ºC) and annealed in N_2 for 180 s.

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Ohmic and Schottky contacts on 3C-SiC epilayers grown by VLS and CVD

Jens Eriksson[1,2 *], Ming-Hung Weng[1], Fabrizio Roccaforte[1], Filippo Giannazzo[1], Raffaella Lo Nigro[1], Jean Lorenzzi[3], Sergey Reshanov[4], Giuseppe Baratta[5], Vito Raineri[1]
[1] *CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy*
[2] *Scuola Superiore – University of Catania, Via San Nullo 5/i, 95123, Catania, Italy*
[3] *LMI, UMR-CNRS 5615, UCBL1, 43 Bd du 11 nov. 1918, 69622 Villeurbanne, France*
[4] *ACREO AB, Electrum 236, SE-16440 Kista, Sweden*
[5] *INAF- Astrophysical Observatory, Catania University, Via S. Sofia 78, 95123 Catania, Italy*
[*] Corresponding author: jens.eriksson@imm.cnr.it

Device applications in cubic silicon carbide (3C-SiC) have long been limited by large defect densities in the available material. Most literature studies concerning devices in 3C-SiC involve epilayers that have been grown on Si substrates. However, the growth of 3C-SiC on Si is complicated owing to the large lattice mismatch (20%) and expansion coefficient mismatch (8% at 475K). Growing 3C-SiC on hexagonal SiC allows an improvement of the crystal quality due to a smaller lattice mismatch (< 0.1%). Growing by a vapor liquid solid (VLS) mechanism further elevates the quality through the suppression of double positioning boundary defects [1]. Consequently, the interest for device applications in 3C-SiC is growing. A fundamental issue for devices is the electrical behavior of metal/SiC contacts, which strongly depends on the 3C-SiC material quality. In this work, Ohmic and Schottky contacts were fabricated on 3C-SiC layers grown either on hexagonal SiC substrates by VLS or chemical vapor deposition (CVD), or on free standing 3C-SiC by CVD.

Good and reproducible Ohmic contacts are crucial for electronic devices, and the properties of the contacts are directly related to the crystal quality of the material. Ni-based Ohmic contacts were formed on doped ($N_D \approx 5\times10^{17}$ cm^{-3}), single-domain 3C-SiC (111) epitaxial layers grown by VLS. The evolution of the electrical and structural properties of the contacts during annealing in the temperature range 600–950°C showed the formation of different nickel silicide phases, accompanied by a gradual reduction of the specific contact resistance ρ_c, eventually settling at values in the range of 1.5×10^{-5} Ωcm^2 [2]. These values are significantly lower than what has been reported for 3C-SiC of similar roughness and doping [3], grown by other techniques, indicating superior crystalline quality of 3C-SiC layers grown by VLS.

Two-dimensional current maps, obtained by scanning 50 × 50 µm^2 areas on the contacts by conductive atomic force microscopy (C-AFM), further revealed that the structural evolution is accompanied by an increased uniformity of the local current distribution as the annealing temperature increases, evidencing that an increase of the effective contact area contributes to the improvement of the contact properties. This is illustrated in Fig. 1 by plotting the evolution of the effective contact area (extracted from the C-AFM current maps) alongside the specific contact resistance, as a function of annealing temperature. This is a new aspect that can help explain the Schottky to Ohmic transition normally observed after high temperature annealing of Ni-silicide/SiC systems in the high doping range [2].

One of the early limitations with the VLS technique is the growth of low doped epilayers, which are required in order to fabricate Schottky contacts. In fact, a major challenge with devices in 3C-SiC is the fabrication of good Schottky contacts. In the past, several metals have been tested as Schottky contact material on 3C-SiC grown on Si, resulting in low Schottky barrier heights (SBHs) [4]. This poor behavior can be related to the high density of defects in the available material. Structural defects can present a current path through the layer which increases the leakage current and reduces the SBH. To study this, the electrical properties of Schottky diodes were investigated as a function of contact area. Reducing the area results in a reduction of the defects under the contact and, as such, we can indirectly relate the influence of defects on the properties of the defined diodes.

Schottky contacts were fabricated on low-doped 3C-SiC epilayers grown by CVD both on hexagonal SiC and on free-standing 3C-SiC. These epilayers have large amounts of stacking faults and twin defects. 100 nm thick, circular Au contacts, ranging in radius from 5-150 µm, were deposited onto the 3C-SiC layers and 100 nm layers of Ni_2Si were deposited as Ohmic back-contacts to form vertical Schottky diodes. The diodes were electrically characterized by current voltage (I-V) measurements in an electrical probe station, as well as by C-AFM. I-V probe measurements were, due to the dimension of the probe tip, limited to the larger diodes of contact radius between 50 and 150 µm. Results from these measurements show barrier heights in the range of 0.6-0.7 eV for both types of structures. The leakage current densities are significantly lower for the diodes on the homoepitaxial 3C-SiC (158 $\mu A/cm^2$ at -1 V) than for those on the 3C/4H-SiC heterostructure (37 mA/cm^2 at -1 V). In the former case, this corresponds to leakage currents in the range of 10 nA for diodes of contact radius 50 µm.
I-V characteristics of diodes of contact radius down to 5 µm were obtained by C-AFM. As the radius is reduced, the characteristics of the diodes gradually improve, as seen from the plot of the SBH vs. contact radius in Fig. 2. For the smallest diodes the SBH approaches the theoretical value for the Au/3C-SiC interface of 1.4 eV. This result demonstrates that the poor behavior of Schottky contacts on 3C-SiC is due to high defect densities. From the yield formula discussed in Ref. [5] and thermionic emission theory, a theoretical model was developed to describe the SBH as a function of defect density. Using the defect density as fitting parameter, a value of 1×10^6 cm^{-2} is necessary to describe our experimental results.
By studying Schottky diodes as a function of contact area, we have shown that the behavior of Au Schottky contacts on 3C-SiC improves dramatically as the amount of defects present under the contact is reduced. Improving the crystal quality, with ensuing reductions of the leakage currents, would allow large area Schottky contacts that can be used to implement e.g. Schottky diode based light detectors. Our results on Ohmic contacts demonstrate that the VLS technique can be used to grow high quality 3C-SiC. Current activities are focused on reducing the residual doping in order to grow low-doped, single-domain layers using this technique.
This work has been supported by EU in the framework of the MANSiC project (Grant No. MRTN-CT-2006-035735).

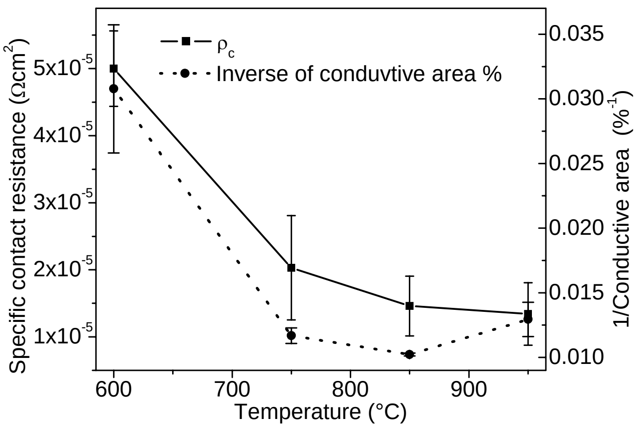

Fig. 1: Specific contact resistance (solid curve), and inverse of the effective contact area (dotted curve) vs. temperature. Measured on Ni-based Ohmic contacts on 3C-SiC grown by VLS.

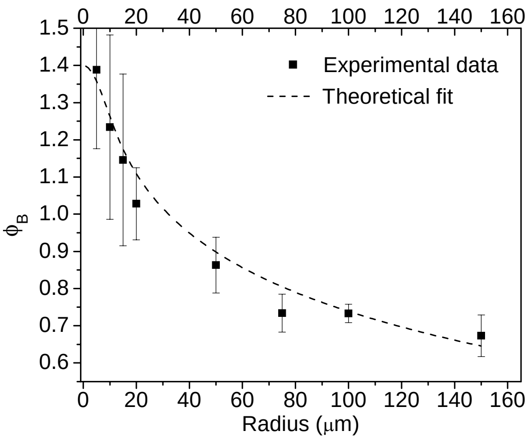

Fig. 2: SBH vs. contact radius, measured on a $Au/3C/4H\text{-}SiC/Ni_2Si$ structure. The dashed curve is a fit to a model that relates the SBH to the defect density.

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Low temperature photoluminescence investigations of 3C-SiC quasi-substrates grown on hexagonal 6H-SiC seeds

G. Zoulis[1*], J. Lorenzzi[2], R. Vasiliauskas[3], N. Jegenyes[2], M. Beshkova[3], S. Juillaguet[1], H. Peyre[1], V. Souliere[2], M. Syväjärvi[3], G. Ferro[2], R. Yakimova[3], J. Camassel[1]
[1] *Groupe d'Etude des Semiconducteurs, CNRS and Université Montpellier 2, cc074-GES, 34095 Montpellier cedex 5, France*
[2] *Laboratoire des Mulitmateriaux et Interfaces, UMR-CNRS 5615, UCBL-Lyon 1, 43 Bd du 11 nov. 1918, 69622 Villeurbanne France*
[3] *Department of Physics, Chemistry and Biology (IFM), Linköping University, SE-581 83 Linköping, Sweden*
[*] Corresponding author: zoulis@ges.univ-montp2.fr

To develop 3C-SiC electronics, the growth of large 3C-SiC substrates with a good crystalline quality and a well controlled level of residual doping is mandatory. In this work, we report the results of low temperature photoluminescence (LTPL) and SIMS investigations performed on 3C-SiC samples grown on hexagonal SiC seeds for quasi-substrates applications. We compare two different techniques: sublimation epitaxy (SE) and vapor-liquid-solid (VLS) epitaxy complemented (or not) by chemical vapour deposition (CVD) and SE. We have found the following.

First, a very low level of residual (nitrogen) doping can be reached using either SE or VLS. Typical LTPL spectra are shown in Fig.1 and, comparing with previous works [1]-[3], we find residual values ranging from ~ 2 to 6 x 10^{16} cm^{-3}. Simultaneously, the residual aluminium concentration can be very low (~5x10^{15} cm^{-3}) which results in a low level of electrical compensation. In most cases, after a CVD re-growth on top of the VLS seeds, the residual level of nitrogen doping does not change significantly but the Al content may change significantly, resulting in higher compensation.

Second, a main p-type character can be found in some SE samples. This departs from previous reports [4] in which the p-type identification was only found from LTPL spectra with strong evidence of donor-acceptor pairs (DAP) transitions. In this work a strong Al-related peak appears in the range of near band-edge excitonic features at ~ 2.365 eV (see Fig.2) which is the usual value [1], [2] reported for the A_0X line in 3C-SiC. All other peaks are phonon replicas and no N-related excitonic line manifests. This is in good agreement with the result of SIMS measurements which show that the Al doping is in the range ~3x10^{17} cm^{-3} while the N one (if any) is below the detection limit of the apparatus (~ 10^{17} cm^{-3}). In some cases, inclusions of 6H-SiC manifest (see insert in Fig.2) which again show a high Al concentration.

Concerning the benefit of hexagonal seeds for quasi-substrates preparation, we have compared the intensity of defect-related lines in the work of Ref.[1] with the results collected in this work. For a sample grown on Si, one should have at least 17 µm thickness to see the peaks corresponding to the interface defects diminishing substantially. On a hexagonal seed, the same is found for thicknesses ~ 5 times lower (~ 2.5 µm).

This work has been supported by EU in the framework of the MANSiC project (Grant No. MRTN-CT-2006-035735).

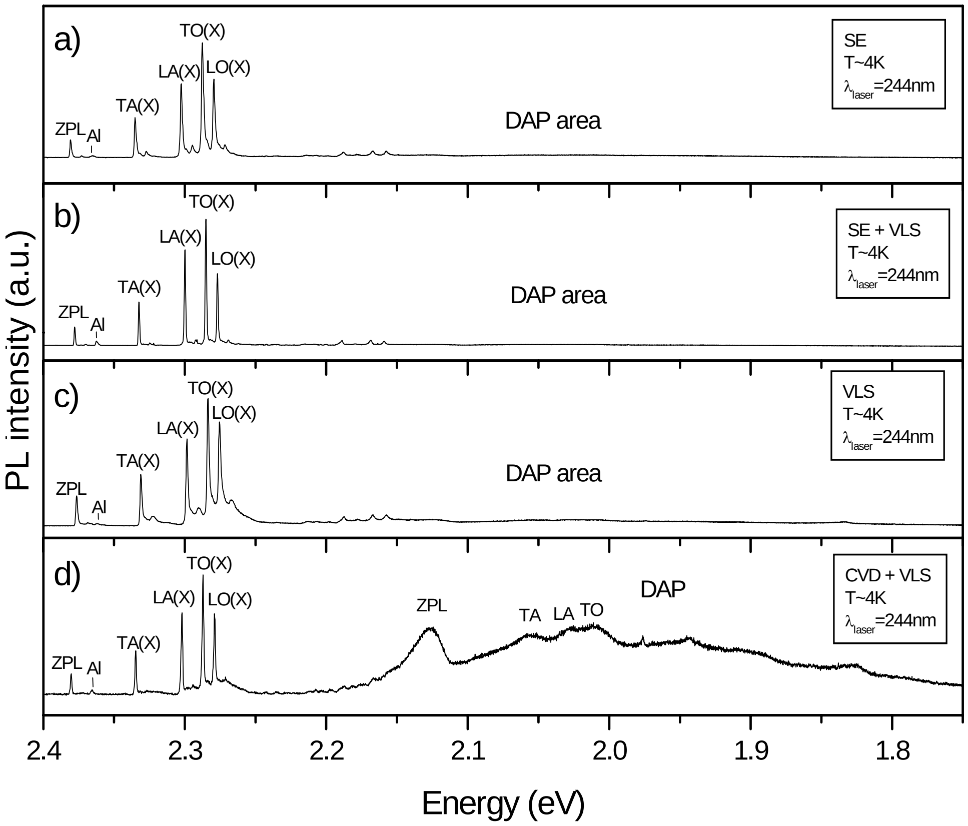

Fig. 1: LTPL spectra collected for different 3C-SiC samples grown using a) SE,b) SE on a VLS seed, c) an optimised VLS technique and d) CVD re-growth on a VLS seed.

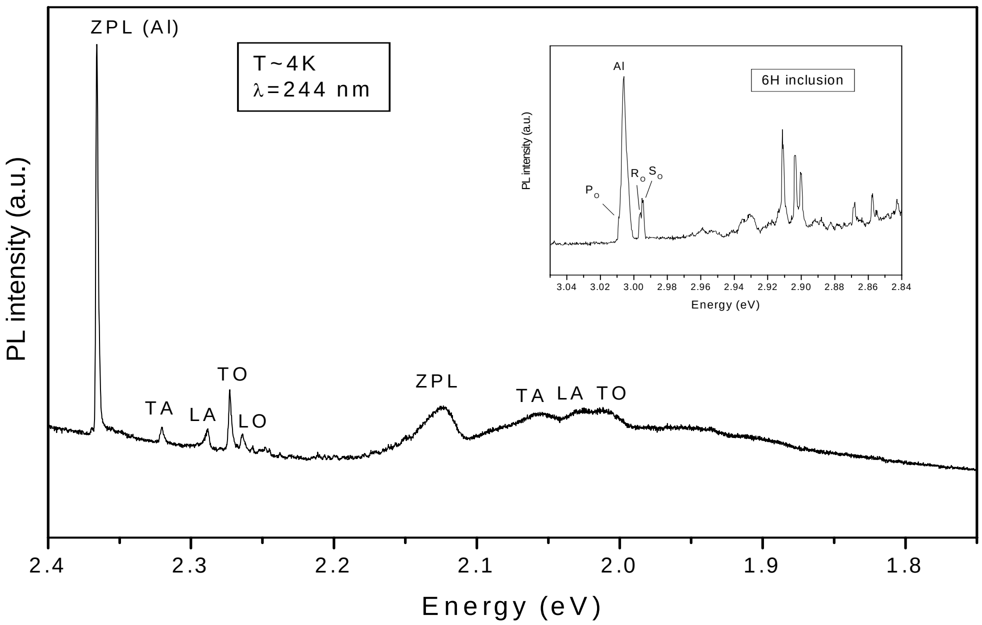

Fig. 2: LTPL spectra collected for an Al-doped sample grown using SE. The first peak corresponds to Al bound excitons. The other ones are one phonon replicas. The insert shows a 6H-SiC inclusion with again a high level of Al concentration.

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Optical diagnostics of 3C/6H heterostructures grown by VLS+CVD techniques

G. Manolis[1*], J. Lorenzzi[2], N. Jegenyes[2], G. Ferro[2], K. Jarašiūnas[1]
[1]*Department of Semiconductor Optoelectronics, Institute of Materials Science and Applied Research, Vilnius University, LT-10222 Vilnius, Lithuania*
[2]*Laboratoire des Multimateriaux et Interfaces, UMR-CNRS 5615, UCB-Lyon1, 43 Bd du 11 nov. 1918, 69622 Villeurbanne, France*
[*] Corresponding author: georgios.manolis@mtmi.vu.lt

Non-linear optical techniques, as free-carrier grating (FCG) and free-carrier absorption (FCA), are among the non-destructive characterization tools suitable for contactless optical monitoring of a semiconductor electronic properties and determination of carrier lifetimes, diffusion coefficients, and diffusion lengths at high excess carrier concentration [1].

In the given work, we investigated non-equilibrium carrier dynamics of differently grown 3C-SiC heteroepitaxial layers on 6H-SiC (0001) on axis Si-face substrates. The 3C layers were produced in two steps: 1) a 3C heteroepitaxial growth using vapour-liquid-solid (VLS) approach and 2) a 3C-SiC homoepitaxial thickening by CVD in order to increase the 3C material to be probed up to 3-8 μm range.

A set of three different 3C-SiC (111) samples was studied at room (RT) and low temperatures (LT). According to the preliminary evaluation of the n-type doping level in the samples by μ-Raman spectroscopy, the VLS-86 sample is the highest doped one ($\geq 10^{17}$cm^{-3}) while SG-125 and VLS-50 are the lowest doped samples ($\leq 10^{16}$ cm^{-3}). In addition, all three samples display a rough surface morphology composed of cube-like facets after CVD growth which is different from the one observed after VLS growth.

Free carrier gratings with various periods Λ were recorded by interference of two 10 ps Nd:YLF laser beams at 351 nm which generated an excess carrier density of $N = 4\times10^{18}$ - 5×10^{19} cm^{-3} within the depth $\alpha^{-1} = 4.5$ μm. The third delayed beam at 1053 nm was probing the grating decay. From the measured FCG decay time τ_G and using the relationship $1/\tau_G=1/\tau_R+1/\tau_D$, we derived the values of ambipolar diffusion coefficient D_α and carrier lifetime τ_R at RT as well as at LT. Complementary measurements of FCA decay provided carrier lifetimes even at higher carrier density, up to 10^{20} cm^{-3} .

In Fig. 1 carrier lifetimes and ambipolar carrier diffusion coefficients are presented as a function of excess carrier density. VLS-50 had an almost constant value of $\tau_R \approx 3.8$ ns. On the other hand, in VLS-86 τ_R increased from 2.6 to 4.4 ns with increasing excited carrier density. We note that τ_R increase at RT is a typical feature of highly excited 3C SiC [3] and points out to saturation of deep carrier trapping centres. In SG-125 layer, the τ_R was constant ($\tau_R \approx 2$ ns) in all excitation range. We note that carrier dynamics in this, rather thin 3-μm layer was influenced by the short lifetime in 6H substrate ($\tau_R \approx 1.1$ ns) since the exciting beam excited both the epilayer and the substrate, Moreover, the observed increase of D_α in SG-125 at low excitations was probably caused by more efficient trapping of electrons and the deviation from carrier plasma bipolarity ($n < p$); consequently, the effective mobility and D_α value increased. Time-resolved FCA measurements on all samples confirmed the measured lifetime values.

In T=40-300K range (Fig.2), the temperature dependence of bipolar mobility (μ_α) revealed typical scattering by ionized impurities at T<100K, especially in the VLS-50 layer. In particular, in T= 40-100K range, the VLS-50 exhibited a strong increase of mobility with increasing the excess carrier density. A similar behaviour was observed in VLS-86, but at smaller extent. We attribute the mobility increase to the filling of deep scattering centers by excess carriers, as the subsequent scattering by neutral impurities became less efficient than by ionized ones. Therefore, comparison of temperature dependencies of mobilities allowed us to suppose that the defect density in VLS 50 is higher than that in the VLS-86 layer.

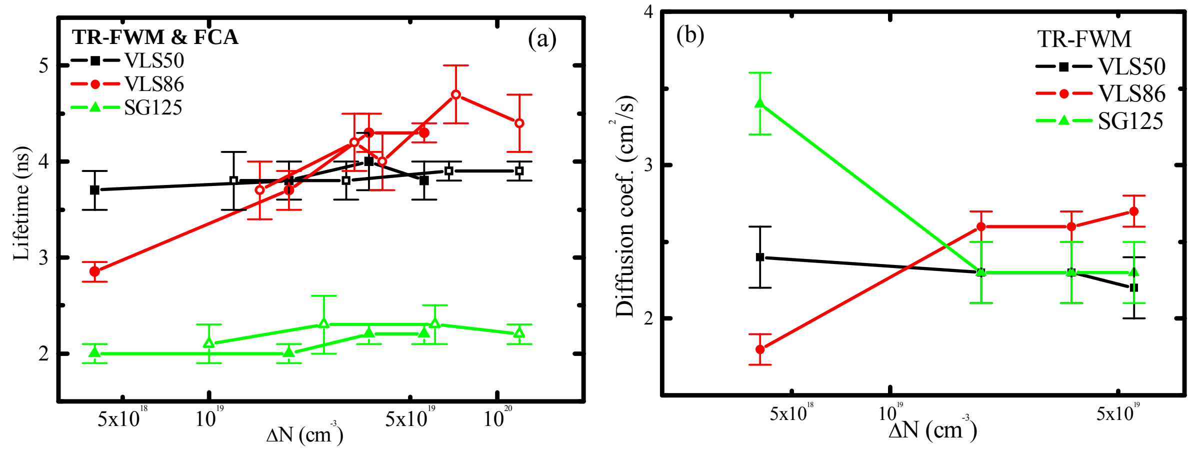

Fig. 1: Carrier lifetime τ_R (a) and ambipolar diffusion coefficient D_α (b) as a function of excess carrier density ΔN at room temperature.

Analysis of FCG kinetics at various temperatures and excitations allowed us to attribute the observed dependencies of μ_α and τ_R to contribution of defects, probably shallow and deeper ones, which became recharged under strong excitation. These defects are acting as nonradiative recombination centres and heat the lattice, as seen from FCG kinetics. At low temperatures and high excitation energies, according to Debye law on specific heat, the thermal gratings were developed and contributed to refractive index modulation simultaneously with the free carrier grating. Assuming that the most pronounced lattice heating is directly connected with the higher defect density, we concluded that VLS-86 layer was less defective than the VLS-50, Moreover, low τ_R value in 3C SG-125 layer as well as in 6H substrate is in line with proposed role of defects.

We acknowledge a support of the research by EC FP6 Contract No. MRTN-CT-2006-35735.

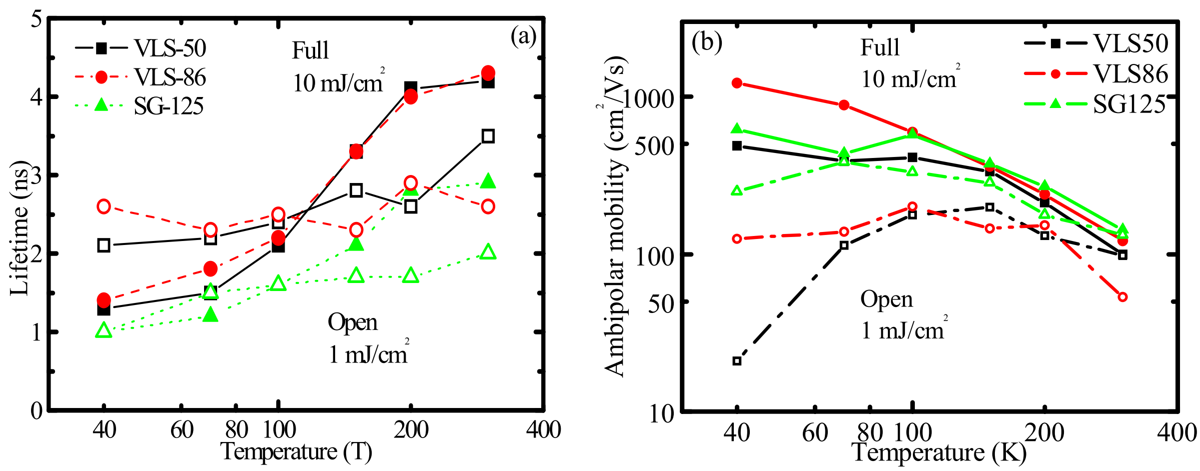

Fig. 2 Temperature dependencies of carrier lifetime (a) and ambipolar mobility (b) at low (1 mJ/cm^2, open symbols) and high (10 mJ/cm^2, full symbols) excitations.

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Structural and electrical characterization for 3C-SiC homoepitaxial layers

M. Kato*, Y. Iwata, Y. Matsushita and M. Ichimura
Nagoya Institute of Technology, Gokiso Showa Nagoya 466-8555, Japan
* Corresponding author: kato.masashi@nitech.ac.jp

Although development of 3C-SiC homoepitaxial layers are indispensable to fabricate 3C-SiC based electronic devices, there have been few reports about 3C-SiC homoepitaxial layers so far [1,2]. In addition, characterization in those reports is not extensive, and detailed characteristics of the layers are not discussed. Therefore, defects which degrade the device performance are still unclear and should be identified by various characterization techniques. In this study, we characterized structural and electrical properties in 3C-SiC homoepitaxial layers using the Raman spectroscopy, etch pit observation after chemical etching, and current-voltage measurements with Ni Schottky contacts.
Samples used in this study were two 3C-SiC homoepitaxial layers grown by chemical vapor deposition on highly doped 3C-SiC (100) bulk substrates, and we named the samples sample A and B. Epilayer thicknesses for sample A and B are 23-30 μm and 28 μm, respectively, while nominal doping concentrations for sample A and B are 4×10^{15} cm^{-3} and 6×10^{16} cm^{-3}, respectively.
Figure 1 shows Stokes Raman spectra for the sample A and B with the (001) backscattering geometry. Both the samples show transverse optical (TO) and longitudinal optical (LO) modes, although the TO mode is forbidden. In addition, sample A shows a folded TO mode, which indicates presence of other polytypes in the crystal. This polytype inclusion would be caused by stacking faults in 3C-SiC. On the other hand, sample B shows a significant background signal, which increases with wavenumber. This background signal may be due to photoluminescence.
In order to observe structural defect distribution, we etched pieces of the samples in KOH at 400°C. The etched surfaces for sample A and B are shown in Figs. 2(a) and (b), respectively. The etched surfaces for both the samples show circular pits and grooves. All the grooves in sample B align in the horizontal direction in the figure. On the other hand, in sample A, some grooves align in the horizontal direction and the rest of grooves are in the vertical direction in the figure. These grooves would originate from stacking faults aligned in [110] and [-110] directions [1]. The groove densities are 1.6×10^{5} cm^{-2} and 1.5×10^{6} cm^{-2} for sample A and B, respectively. Therefore sample B has one order of magnitude larger density of stacking faults than sample A.
The Ni Schottky contacts evaporated on the sample A and B show rectification properties expected for an n-type semiconductor. Figure 3 shows a histogram of leakage current densities at -5V for the contacts on sample A and B. Most of the contacts on sample A show leakage current of the order of 10^{-4} A/cm^2, while those on sample B show leakage current in a range of 10^{-1} to 10^{-3} A/cm^2 at -5V. Therefore leakage current is higher and scattered for the contacts on sample B. Sample B has one order of magnitude larger doping concentration and stacking fault density than sample A. These results suggest that the lower doping concentration and stacking fault density lead to better electrical characteristics for homoepitaxial 3C-SiC layers.
This work is partly supported by the Research Foundation for the Electrotechnology of Chubu.

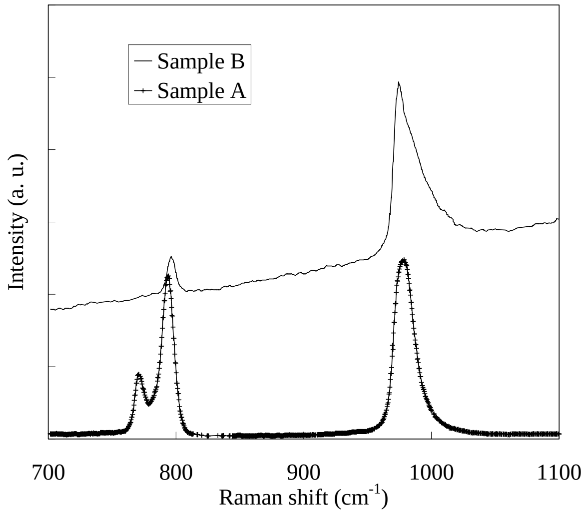

Fig. 1. Raman spectra for the samples.

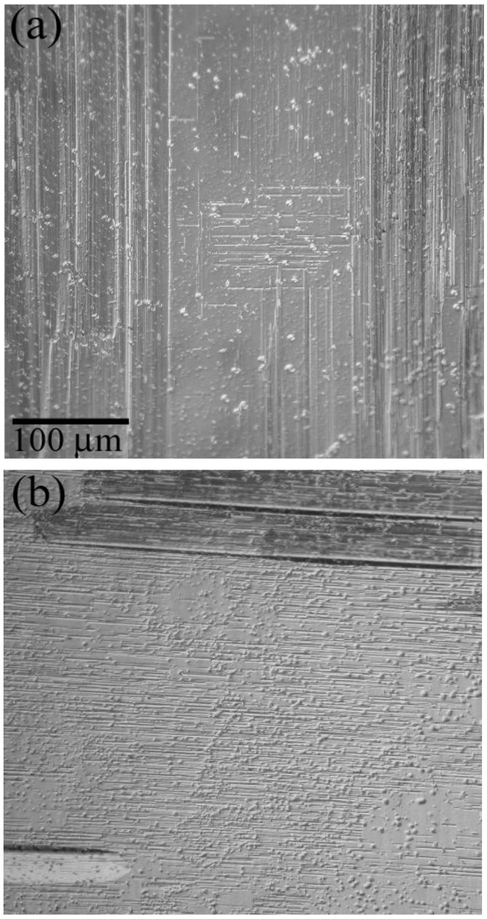

Fig. 2. Optical micrographs for etched surfaces: (a) sample A, and (b) sample B.

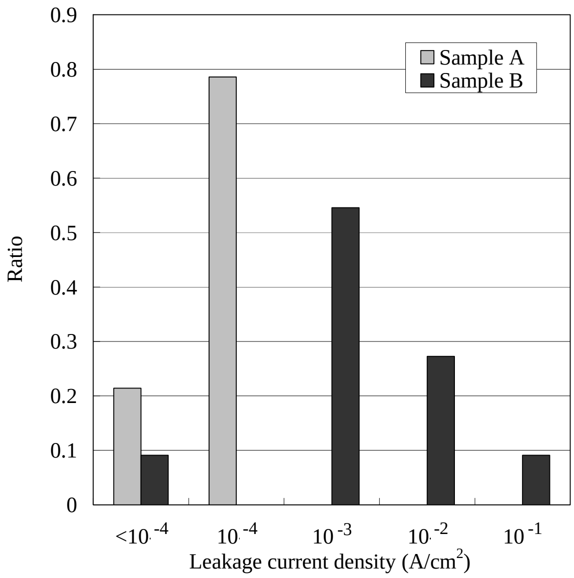

Fig. 3. Histogram of leakage current densities at -5V for Schottky contacts on the samples.

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Comparative study of oxides on n-type free standing 3C-SiC (001)

R. Esteve[1,2,*], A. Schöner[1], S.A. Reshanov[1], C.-M. Zetterling[2], H. Nagasawa[3]
[1]*ACREO AB, Electrum 236, SE-164 40 Kista, Sweden*
[2]*Dept. Information and Communication Technology, KTH, Electrum 229, SE-164 40 Kista, Sweden*
[3]*Hoya Corporation SiC Development Center, 1-17-16 Tanashioda, Sagamihara-shi, Kanagawa 229-1125, Japan*
[*] Corresponding author: romain.esteve@acreo.se

Alternative ways to improve the oxidation process of free standing 3C-SiC (001) were developed and tested with the aim to reduce the fixed and mobile charges in the oxide and at the SiO_2/3C-SiC interface.
At first we focused on the improvement to thermally grown oxides (see Table 1) by studying the influence of the growth temperature on the dry oxidation of 3C-SiC (samples ox 1 and ox 2). In a second approach we assessed the oxide quality improvements by implementing low temperature post oxidation steps. Thermally grown oxides were post oxidized in wet (ox 3) and dry (ox 4) oxygen in order to investigate stabilization and hydrogen passivation of active defect centers in the oxide or at the SiO_2/3C-SiC interface. Finally, the efficiency of nitridation has been studied by thermal oxidation of 3C-SiC using N_2O (samples ox 5 and ox 6). The wet post oxidation annealing of N_2O oxidized 3C-SiC has been investigated (ox 7) as well.
The standard dry oxidation at 1100 °C results in a high negative flat band voltage of -31 V and in a high interface state density $D_{it} = 4.3\times10^{13}$ eV^{-1}cm^{-2}. The temperature increase up to 1200°C slightly reduces the fixed charge in the oxide at the cost of an increase in D_{it} and surface potential fluctuations. Thus it did not result in an improvement of the oxide on 3C-SiC. A strong reduction of both the fixed charge and the D_{it} can be achieved by appying a post oxidation annealing step. MOS capacitors fabricated by N_2O oxidation revealed a large hysteresis in depletion.
We established an advanced oxidation process combining a plasma enhanced oxide deposition (PECVD) step with a rapid post oxidation step (see Table 1). The post oxidation step performs a densification of the deposited oxide and a thermal oxidation of a 3nm to 5nm thin layer of SiC. Three gas atmospheres (N_2O, dry and wet oxygen) have been studied for the post oxidation step (samples dep 1-3) and are compared to the post anneal in N_2 (dep 4 and 5). The measured C-V, G-V, and I-V curves as well as the energetic distribution of D_{it} for the deposited oxides are exemplarily shown in Figs. 1 and 2. We could demonstrate that using wet oxygen conditions is beneficial for the post-oxidation step of n-type 3C-SiC. MOS capacitors fabricated using wet post oxidation show a reduction in flatband voltage shift, effective oxide charge density (see Fig. 1(a) and Table 1), and density of interface traps (see Table 1 and Fig. 2(a)), as well as an increase in the oxide breakdown field (see Fig. 2(b)). Hydrogen provides an efficient passivation of charges and a saturation of interface states. The advanced oxidation process combining oxide deposition and wet post-oxidation is superior to the other tested processes in the case of n-type 3C-SiC.
The inefficiency of nitridation for the improvement of the oxide quality on 3C-SiC has been investigated (see Table 1). MOS capacitors fabricated by N_2O thermal oxidation or post oxidation processes revealed the formation of deep interface states (see complex structure of the conductance peak of sample dep 1 in Fig. 2(b)), which are possibly nitrogen related, while the effective oxide charge remained comparable to the one for dry oxygen post oxidized MOS capacitors.
The support of this work by the EC through the MANSiC project (Marie Curie Action MRTN-CT-2006-035735) is gratefully acknowledged.

Table 1. Processing parameters and resulting density of interface traps (D_{it}) and effective oxide charge (Q_{eff}) of investigated MOS capacitors.

sample	oxidation/deposition gas species	T(°C)	annealing gas species	T(°C)	D_{it}* (10^{12} cm^{-2}eV^{-1})	Q_{eff}/q (10^{12} cm^{-2}eV^{-1})
ox 1	O_2	1100	—	—	42.7	9.3
ox 2	O_2	1200	—	—	65.9	7.1
ox 3	O_2	1100	O_2	950	7.1	1.3
ox 4	O_2	1100	O_2:H_2 (1:1)	950	5.2	0.9
ox 5	N_2O:N_2 (1:4)	1200	—	—	11.5	3
ox 6	N_2O:N_2 (1:4)	1250	—	—	9.1	3.1
ox 7	N_2O:N_2 (1:4)	1250	O_2:H_2 (1:1)	950	9.4	1.6
dep 1	SiH_4:N_2O	300	N_2O:N_2 (1:4)	1100	5.1	2
dep 2	SiH_4:N_2O	300	H_2O	950	1.9	0.2
dep 3	SiH_4:N_2O	300	O_2	950	2.6	1.7
dep 4	SiH_4:N_2O	300	N_2	1100	7.8	4.6
dep 5	SiH_4:N_2O	300	N_2	950	2.4	2.6

*D_{it} determined at E_C-E_{it} ≈ 0.63 eV

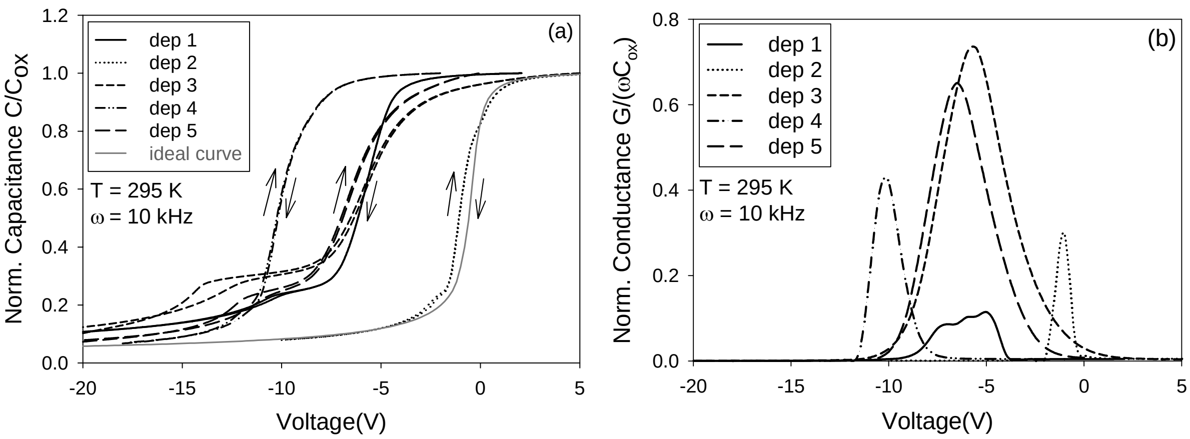

Fig. 1. Normalized C-V (a) and G-V (b) curves taken on 3C-SiC MOS capacitors fabricated by PECVD with post oxidation in N_2O (1100°C), wet, and dry oxygen (950°C) for 3 hours (dep 1-3) or post annealed in N_2 at 950°C and 1100°C for 3 hours (dep 4 and 5).

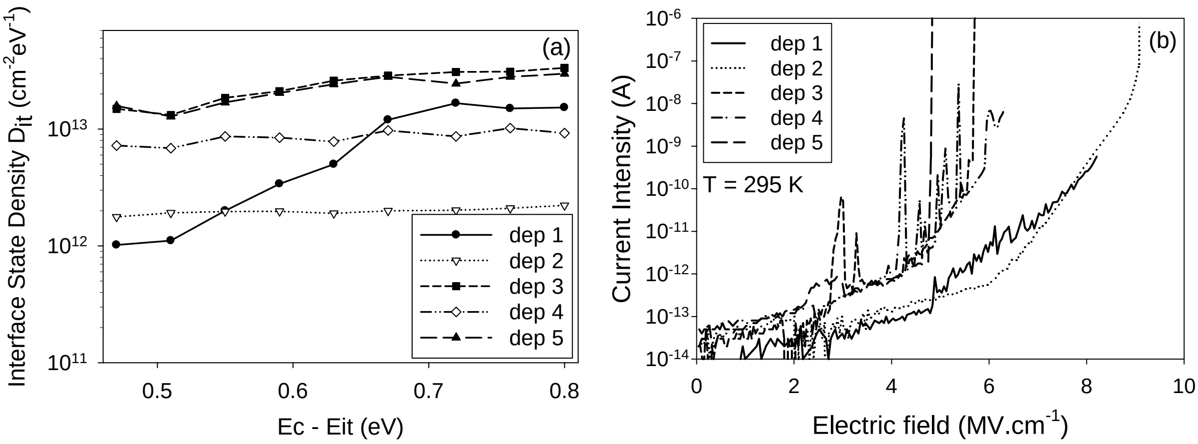

Fig. 2. Interface state density D_{it} as a function of the energy position (a) and I-V characteristics (b) of 3C-SiC MOS capacitors fabricated by PECVD and post oxidized in N_2O (1100°C), wet, and dry oxygen (950°C) for 3 hours (dep 1-3) or post annealed in N_2 at 950°C and 1100°C for 3 hours (dep 4 and 5).

Sensors on 3C-SiC

A. Lloyd Spetz *, K. Buchholt, M. Andersson, M. Syväjärvi, V. Khranovskyy, R. Yakimova
Dep. of Physics, Chemistry and Biology, Linköping University, SE-581 83 Linköping, Sweden
* Corresponding author: spetz@ifm.liu.se

Wide band gap, WBG, materials like SiC, GaN/ GaAlN, AlN, ZnO and Diamond perform the basis for multifunctional bio and chemical sensors. For example SiC devices based on 4H SiC have been operated up to 1000°C and proven to withstand harsh environment like exhaust gases and flue gases, see Fig. 1. An ammonia sensor for control of SCR, selective catalytic reduction, in diesel exhaust was demonstrated [1], while a SiC based sensor system for control of the combustion in wood fuelled household boilers (burners) is being commercialized [2]. For operation of SiC based gas sensors at temperatures above 400°C we have started a development of new contact materials [3]. NO / NO_2 (NO_x) sensors are of great interest for numerous environmental purposes. For example the SCR process may also be controlled by a NO_x sensor, however, the operation temperature should preferably be above 400°C. We have investigated Au and Pd nanoparticles as sensing layers in FET devices. Au nanoparticles show an increased response to NO and NO_2. Pd showed an interesting fractal particle formation and also increased sensitivity to NO. However, the operation temperature is limited to about 300°C for Pd and even lower for Au [4]. The ZnO material exhibit potential as multisensors, since FET, resonating devices and also resistive sensors are realized. We have compared the resistivity change due to oxygen of sensing layers based on ZnO nanoparticles or ZnO films [5]. Furthermore, we have investigated the resistivity change of Ga doped ZnO nanoparticles to NO_2 and compared that to undoped material. We found an increased stability and reproducibility in the response to NO_2 even at an operation temperature of 550°C [6].

Recent progress in 3C SiC material properties has made this an interesting alternative to other SiC polytypes for chemical sensors. Neudeck et al fabricated p^+n-junction diodes on 3C SiC on step free 4H SiC [7]. The electrical characteristics in reverse mode show excellent low-leakage behaviour, below previous 3C-SiC devices produced by other growth techniques. The estimated breakdown field of 3C-SiC is higher than twice the breakdown field of silicon, but only around half the breakdown field of <0001> 4H-SiC for the doping range studied. Hunter et al report that the development of a sensor array to detect the concentration of fuels like hydrogen, hydrocarbons, or hydrazine as well as oxygen is necessary for a range of applications like for space crafts [8]. Work is performed to develop an integrated smart leak detection system based on miniaturized sensors to detect hydrogen, hydrocarbons, or hydrazine, and oxygen. The approach is to implement intelligent Microelectromechanical Systems (MEMS) based sensors systems with signal conditioning electronics, power, data storage, and telemetry. It will be interesting to process devices using 3C-SiC as the bulk material for sensors.

3C SiC also shows interesting potential as a thermistor material. SiC thin film thermistors for the range 0-500°C has been demonstrated [9] and ultra-high purity polycrystalline CVD-SiC for the range 25-365°C [10]. We have studied both 4H SiC and 3C SiC as thermistor material up to 600°C and 3C SiC in the temperature range RT to 750°C, see close up between 580 - 750°C in Fig. 2. Since the resistivity still is 600 Ohm at 750°C for a component, which is not optimized as a thermistor, this shows that 3C SiC has the potential to reach even higher temperatures. Long term stable ohmic contacts, which are needed for the measurements will have to be developed. We intend to test the same approach as for the 4H SiC sensor material above. A challenging task will be to process transistor devices integrated with resistivity changes in sensing layers and a thermistor for temperature control.

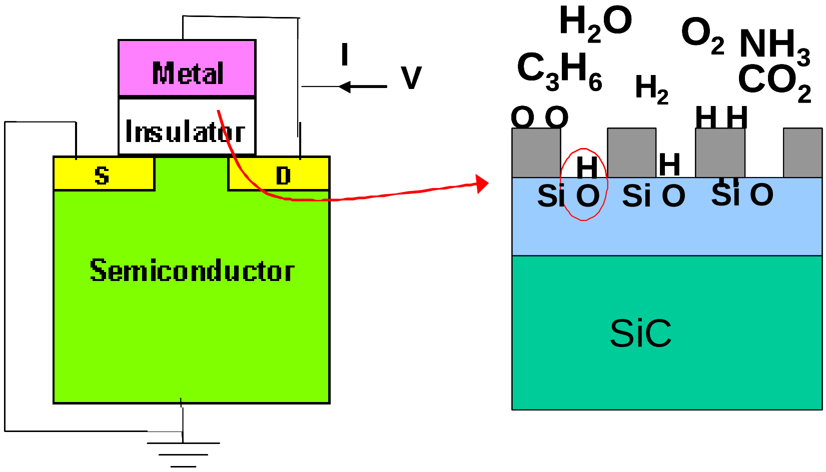

Fig. 1: Schematic picture of a field effect transistor as asensor device and a close up of the gate area (to the right). Charging of the gate area by gas molecules create an electric field which changes the current through the transistor.

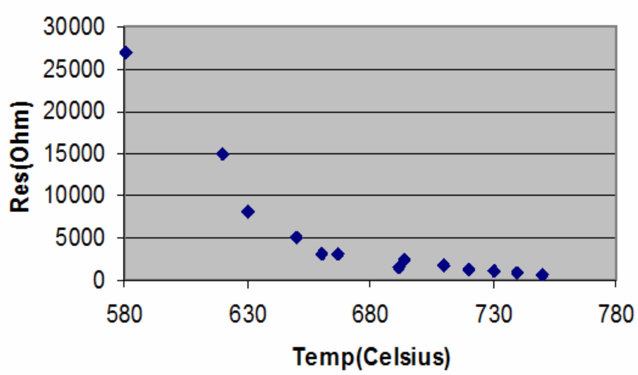

Fig. 2: 3C-SiC as a thermistor material. Measurements in the oven for temperature over 580°C.

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Polycrystalline 3C-SiC films deposited on 100 mm Si wafers for MEMS

A. Poggi[1,*], A. Schöner[2], A.Roncaglia[1], F. Mancarella[1], S. Milita[1], M. Bellei[3]
[1]*CNR-IMM sezione di Bologna, Via Gobetti 101, 40129 Bologna, Italy*
[2]*ACREO AB-Electrum 236, Isafjordsgatan 22, SE-164 40 Kista, Sweden*
[3] *Medica s.r.l., Via degli Artigiani 6, 41036 Medolla- Modena , Italy*
[*] Corresponding author: poggi@bo.imm.cnr.it

Silicon Carbide (SiC) is an attractive material to substitute Si in microelectromechanical systems (MEMS) for harsh environments. In particular polycrystalline cubic SiC (3C-SiC) is of growing interest due to the possibility of being deposited on a variety of technologically relevant substrates, such as Si, SiO_2, and Si_3N_4. Thus the process freedom is increased, especially for surface micromachining.
In this work we evaluate the properties of polycrystalline 3C-SiC films grown heteroepitaxially on 100 mm Si (100) wafers. The films were grown in a commercially available hot wall CVD reactor equipped with wafer rotation. Silane and propane diluted in hydrogen were used as growth precursors, and pure nitrogen gas for doping. The growth process was done at a growth temperature of 1375 °C and a pressure of 70 mbar. It was divided into two steps. First a high nitrogen doped buffer layer was grown on top of the Si substrate and then a low nitrogen doped film was grown on the buffer layer. For the investigations, two thicknesses of the low doped film were chosen: 1.5 µm and 15.0 µm. The growth rates of the thinner and the thicker film were 2 µm/h and 4 µm/h, respectively.
The grown 3C-SiC films have been characterized structurally, chemically and mechanically. X-ray diffraction (XRD) measurements revealed that the films are formed by polycrystallites of 3C-SiC, whose texturing depends on the film thickness. The analysis of the diffracted intensity of the different reflections and comparing them to the theoretical values result in a preferential orientation of the crystallites with (200), thus laying parallel to the surface, while in the thicker film the 3C-SiC crystallites are (220) textured (see Fig. 1). The surface morphology of the films was characterized by scanning electron microscopy (SEM). SEM pictures of the 1.5µm and 15µm films are shown in Fig. 2. Independent of the thickness, the surface looks as formed by small-sized crystallite aggregates, but the thicker film has larger aggregates than the thinner film. The different texturing and surface morphology of the two poly-SiC films have to be carefully considered for the investigations, because the mechanical properties, such as Young's modulus and the residual stress, are strongly affected by the size of the crystallites. This is crucial for MEMS applications.
The planar average residual stress on both films was estimated by the wafer curvature technique. A standard stylus profiler was employed for the profile measurements. For consistency check, the curvature measurements were repeated and confirmed by XRD. The stress extraction was performed by Stoney's formula on the 1.5 µm-thick film. For better accuracy, finite element modeling was employed for the stress extraction of the 15 µm-thick film, by assuming a Young's modulus and Poisson's ratio for the SiC film of 400 GPa and 0.16, respectively. The extracted stress values were 740±25 MPa for the thinner film and 480±40 MPa for the thicker one. The difference in stress values for the two film thicknesses is currently under further investigation.
The chemical inertness to several commonly used etchants (KOH, TMAH, HF-based solutions) was verified for both film thicknesses; the 3C-SiC layers were completely not etched, indicating that the films were continuous and free of pinholes.
By rear side bulk anisotropic Si etching, the SiC films of both thicknesses were released creating poly-SiC diaphragms ranging in size from 0.5x0.5 mm^2 up to 1x1 mm^2. All diaphragms were flat confirming a tensile residual stress in the 3C-SiC films. A nominally 1.5µm thick poly-SiC film was employed to fabricate cantilevers, bridges, strain gauges,

double ended tuning fork resonant force sensors and suspended inertial masses using a front side micromachining process. Fig. 3 shows a group of free standing cantilevers with a length ranging from 10 µm to 300 µm and bridges with a length of 10 µm to 320 µm. All the beams are 4 µm wide. For increasing length, the cantilever bending increases indicating the presence of a significant stress gradient in the film. The absence of deformation observed on bridge structures confirms a tensile residual stress in the 1.5µm thick 3C-SiC films.
The achieved results demonstrate the potential of the technology based on polycrystalline 3C-SiC films of high robustness with comparably low production cost (growth on large area Si wafers) for MEMS applications.

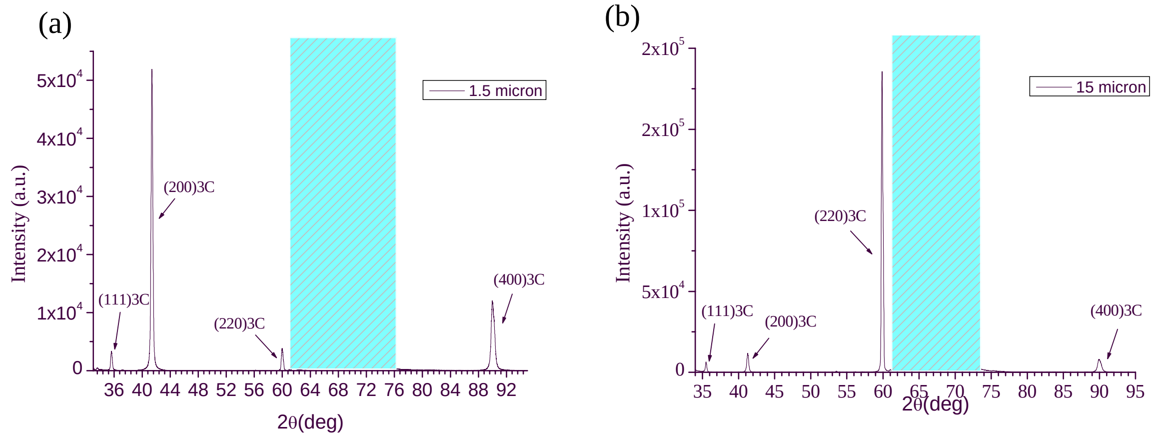


Fig.1: XRD patterns recorded in specular geometry (θ/2θ scan) for (a) a 1.5 µm and (b) a 15 µm, 3C-SiC film.

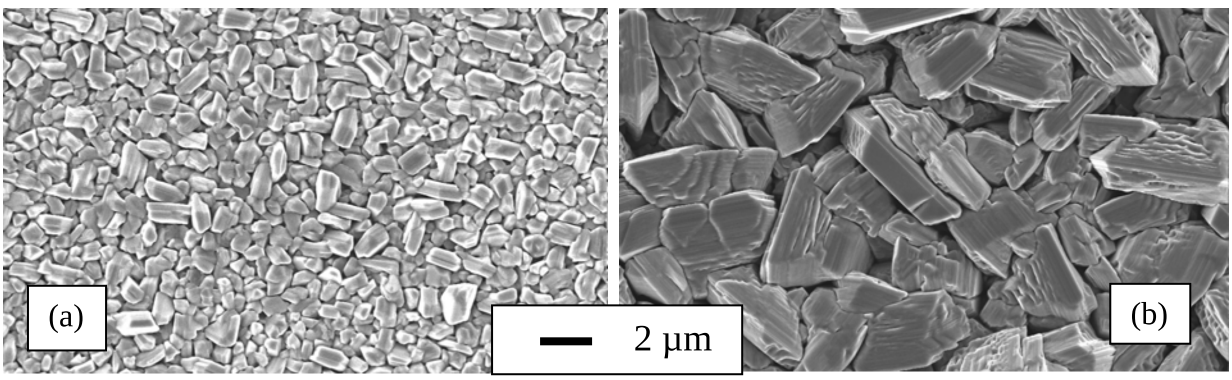


Fig.2: SEM micrographs of poly 3C-SiC films with thicknesses: (a) 1.5 µm and (b) 15 µm.

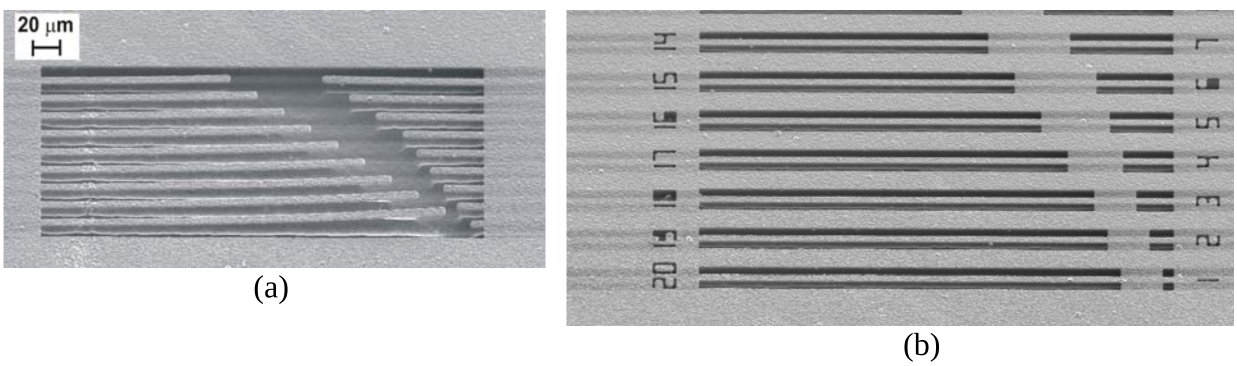
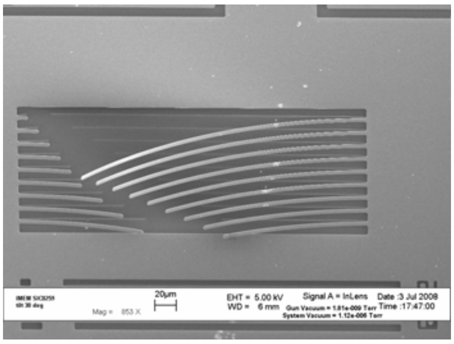


Fig.3: SEM micrographs of (a) cantilevers and (b) bridges from poly 3C-SiC 1.5 µm thick films

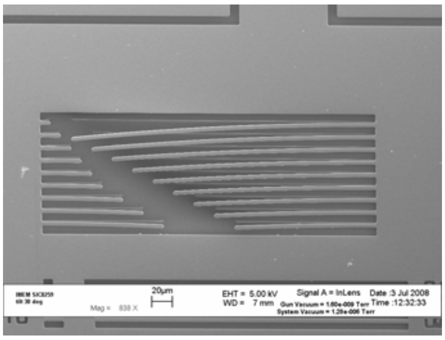
Stresses in SiC MEMS test structures

M. Bosi[1*], G. Attolini[1], B.E. Watts[1], C. Frigeri[1], F. Rossi[1], A. Poggi[2], A. Roncaglia[2], F. Mancarella[2], V. Hortelano[3], O. Martinez[3]
[1]*IMEM-CNR, Viale delle Scienze 37/a, 43100 Parma, Italy*
[2]*IMM-CNR, Via Gobetti 101, 40129 Bologna, Italy*
[3] *GdS-Optronlab, Dpto. Física de la Materia Condensada, Edificio I+D, Universidad de Valladolid, Paseo de Belén, 1, 47011 Valladolid, Spain*
[*] Corresponding author: bosi@imem.cnr.it

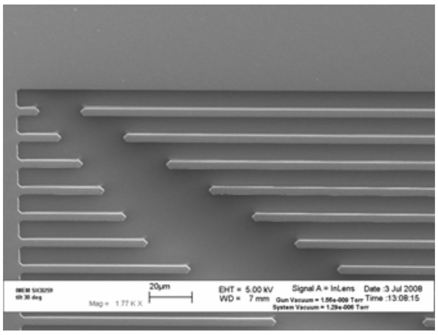
The CVD deposition of SiC/Si was performed in a home built, horizontal, cold-walled reactor, using induction heating. The precursors used were C_3H_8 and SiH_4 both diluted to 3% in hydrogen. The growth was performed on HF etched 2" silicon substrates and consisted of a thermal treatment at 1000 °C, a carburisation of the Si surface under propane while ramping from 400 to 1100 °C with 5 minutes at 1100°C in C_3H_8 flow, and finally SiC film growth at 1200 °C using both propane and silane for 10 minutes. We observed a thickness gradient from the front to the back end of the wafer, ascribed to a depletion of reactants in the gas phase.
The test structures were released either by a wet etch of the Si substrate to produce membranes or by a dry etch of the SiC epilayer to reveal cantilevers.
In Fig. 1 several cantilevers, obtained in different positions of the same SiC sample and with different thickness (indicated), show a different degree of bending.
The upward curvature of the cantilever structures indicates the presence of a strain gradient through the SiC layer that changes with thickness, becoming undetectable in the thickest film. On the other hand, observation on beam structures (anchored by both side to the substrate) shows that for the thickest films the residual average strain is compressive.
A typical Raman spectrum obtained on a freestanding "flat" membrane shows the TO and LO peak being located at 795±1 cm^{-1} and 966±2 cm^{-1}, respectively, depending on the position on the membrane. A typical Raman spectrum on a flat membrane is presented in Fig 2a. The results of the peak fittings of both TO and LO bands for different points along the membrane were used to calculate the strain values ($\Delta a/a$) for each position in the sample, using the linear relations of Olego and Cardona [1]. The obtained $\Delta a/a$ values are presented in the Fig. 2b and a difference between the TO and LO is observed, although the fluctuations trends are the same. This shows that there is a small contribution of tensile strain on the peak shift at the different points of the suspended structure, coherent with the fact that the membrane is flat and not buckled. On the other hand, the stronger redshift and $\Delta a/a$ value for the LO peak is ascribed to the relaxation of the Raman selection rules due to lattice defects, which for the LO phonon band are more marked.
The control of the growth conditions, particularly of the propane concentration, permitted to reduce the stress in the film, even if residual strain gradients could not be avoided as observed in freestanding structures such as cantilevers. The strain gradient diminishes as the film became thicker and it was possible to release un-deformed cantilevers in certain areas of the sample.
In conclusion, different types of MEMS test structures have been fabricated using β SiC films grown on silicon. A gradient of strain has been evidenced by the fabrication of cantilevers. Raman spectra obtained on flat membranes show the presence of tensile strain and reveal lattice defects, because the Raman selection rules are relaxed.



400 nm



800 nm



1000 nm

Fig.1: Cantilevers obtained in different zones of the same SiC film with different thickness

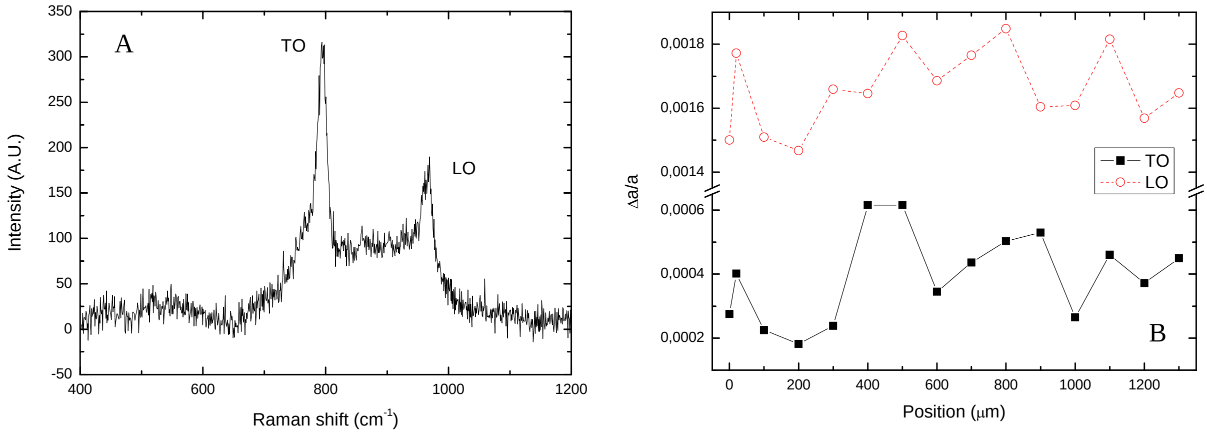


Fig.2: Typical Raman spectrum obtained on a freestaing membrane (A). Strain values obtained from Raman fittings in different point of the freestaing membrane (B)

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Novel high-*k* gas sensors for silicon carbide technology

M.H. Weng[1,2*], R. Mahapatra[1], N.G. Wright[1], A.B. Horsfall[1]
[1] *School of EECE, Newcastle University, Newcastle upon Tyne, NE1 7RU, United Kingdom*
[2] *Present address: CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy*
[*] Corresponding author: minghung.weng@imm.cnr.it

The desire to deploy solid-state sensors and electronics in applications, which have unavoidable exposure to intense radiation, corrosive gases and high temperatures, is of great interest for many scientists and engineers. The excellent material properties of SiC coupled to the high strength of the Si–C bond offer new possibilities for developing hostile devices for more challenging applications than those possible with Si devices. Of the major classes of SiC based sensing electronics, one potential type of SiC sensor is the gas detector, typically based on a capacitor with a catalytic contact. The present work reports a novel approach of Metal-Insulator-Semiconductor devices based on Silicon Carbide technology (MISiC), which have been examined for their ability to deploy in extreme environments.
Research grade N-type 4H-SiC wafers of 10 µm thick epilayer doped with 3 x 10^{15} cm^{-3} were used to fabricate metal-insulator-semiconductor capacitors. The 4H-SiC wafers were cleaned using trichloroethylene (TCE), acetone, isopropyl alcohol (IPA) followed by rinsing in deionised (DI) water. After that a conventional RCA clean was carried out, and then the wafers were dipped in to a diluted HF solution to remove native oxide on the SiC surface prior to oxidation. Thermal oxides of 25 nm thickness were grown at 1150ºC in dry O_2 ambient prior to titanium (Ti) deposition. Titanium films of 50 nm thickness were deposited on SiO_2/SiC stack layers using a thermal evaporation system at the base pressure of 5 x 10^{-6} torr. Ti-films were then oxidized in dry O_2 ambient at temperature 800 ºC to form 75 nm thick TiO_2 layers. Subsequently, 50 nm palladium (Pd) layers were deposited and patterned as a gate electrode of different areas to fabricate MISiC capacitors. The schematic structure of the sensor is illustrated in figure 1.
The MISiC high-*k* capacitor structure is ideal for the manufacture of small, lightweight sensors for robust applications. MISiC gas sensors were tested in nitrogen (N), hydrogen (H_2), oxygen (O_2) and hydrogen sulphide (H_2S) ambient at a range of temperatures up to 600°C. Figure 2 shows a comparison of the characteristics of the sensor in hydrogen, oxygen and hydrogen sulphide ambient. The response of the sensor to H_2S is lower than that of the hydrogen, although they are both controlled by the formation of the charge dipole layer. This indicates that the catalytic decomposition of H_2S on the palladium is incomplete and not all the hydrogen from the molecules is converted to an atomic form. It can also be observed that exposure to oxygen gives a response which is opposite to that for hydrogen containing gases, with a reduction in leakage current on exposure. The sensor response can be monitored by the leakage current through the device which is described by a trap assisted conduction mechanism. The model is simplified and described in the work of Fiorenza [1] as following equation,

$$J_L = C_1 E \exp\left(\frac{-q\phi_A}{kT}\right)$$

Where C_1 is related to the density of trapping states in the bulk of the dielectric, E the electric field in the dielectric stack and ϕ_A is the barrier height of the palladium / TiO_2 junction as shown in figure 3. This mechanism is only applicable for low electric fields and so only low voltages (corresponding to a maximum electric field of 50 kV cm^{-1}) have been investigated here. The barrier height (ϕ_A) between the metal contact and the insulator changed on exposure to different gas species. The value was extracted to be 0.405eV for nitrogen, 0.325eV in

2000ppm H_2, and 0.505eV in 1800ppm O_2. The response to H_2S is observed to be hydrogen-like with a smaller change in barrier height than for pure H_2, which we describe by incomplete dissociation of the molecule on the catalyst surface. The sensor response in H_2S is also strongly dependent to the oxygen concentration in the mixture, which is explained by the use of a Claus reaction [2]. To conclude, the response to hydrogen and oxygen is shown in figure 4. This reduction in barrier height with hydrogen can be explained by the formation of a charge dipole layer located immediately under the catalytic gate contact, as has been observed in Schottky based gas sensors [3]. The increase in barrier height with oxygen has two possible explanations. The decomposition of oxygen molecules forms oxygen ions, which either creates a negative charge dipole layer under the gate metal [4], or oxidizes any remaining hydrogen ions to form water and leave the interface uncharged [5].

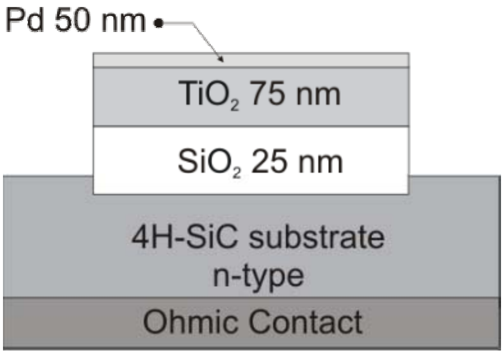

Fig. 1: Schematic cross section of a capacitive gas sensor.

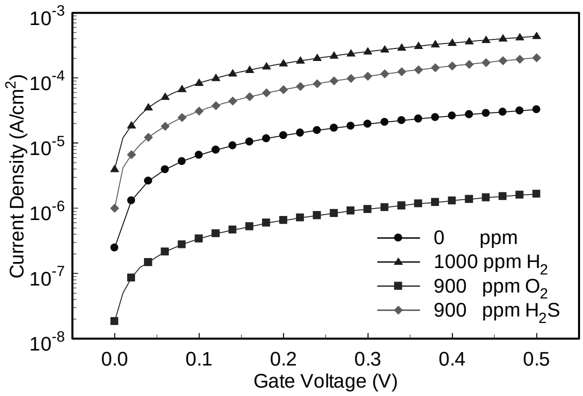

Fig. 2: Responses in different gases at 325°C.

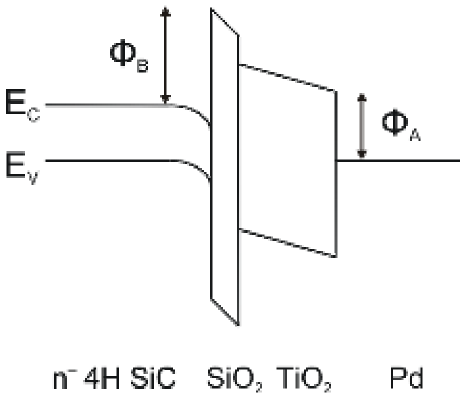

Fig. 3: Band diagram showing the barrier heights ϕ_A and ϕ_B.

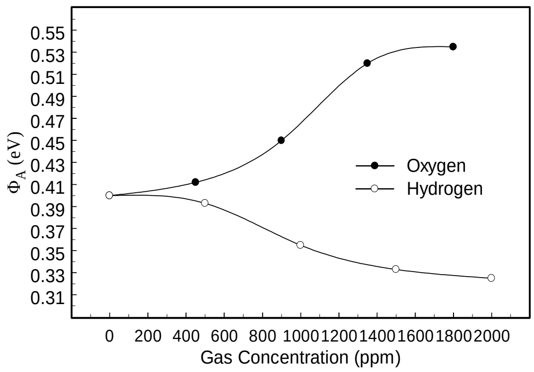

Fig. 4: Variation in barrier height with hydrogen and oxygen exposure.

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Towards high performant UV detectors in SiC

A. Sciuto [1*], F. Roccaforte [1], M. Mazzillo [2], V. Raineri [1]
[1] *CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy*
[2] *ST Microelectronics, Stradale Primosole 50, 95121, Catania, Ital*
* Corresponding author: antonella.sciuto@imm.cnr.it

The detection of the ultraviolet (UV) radiation from the Sun, from astronomical objects, or from artificial sources has received a great attention in the last years, particularly for applications where the insensitivity to the visible component of the light ("solar blindness") is required (UV astrophysics, dermatology, industrial flame detection, etc.). Due to their wide band gap, hexagonal silicon carbide polytypes (4H-SiC, 6H-SiC) are excellent candidates for UV "solar blind" detection. Moreover, among SiC polytipes, they have the already reached an excellent crystalline quality, suitable for electronic device fabrication. PiN diodes on SiC for UV-detectors with promising performances and ultraviolet-visible rejection ratio of about 100 are typically fabricated. However, in order to enhance the sensitivity at short wavelengths, Schottky diodes are preferred to PiN diodes, as the carrier generation occurs in the space-charge region, i.e., at the semiconductor surface, thus allowing a high built-in electric field. Furthermore, as majority carrier devices, Schottky diodes guarantee a faster response than p-n junctions. Finally, Schottky diodes involve a simpler fabrication processes than PiN structures. The conventional Schottky-type UV detectors use "semitransparent" thin metal layers (around 20 nm thick) with high values (1.4-1.8 eV) of the Schottky barrier on SiC (Ni, Au, Pt,….). However, the sensitivity of these devices falls at low wavelengths (below 250 nm), due to the low penetration depth of the UV radiation in the metal. Even if the quantum efficiency of SiC detectors can be improved by further reducing the thickness of the semitransparent metal film (up to few nm), this approach can lead to a non-uniform Schottky barrier and be detrimental for the mechanical and thermal stabilities of the contact. In order to overcome this limitation, we demonstrated a vertical Schottky-type UV detector on 4*H*-SiC based on the "pinch-off" surface effect [1], obtained by means of a self-aligned nickel silicide (Ni_2Si) interdigit semitransparent contacts. These Schottky-type photodiodes were fabricated on n-type 4H-SiC epitaxial layers, few micrometer thick with a dopant concentration of the order of 10^{15} cm^{-3} . Ohmic contacts on the sample back side was formed by evaporation of a Ni film, followed by an annealing at 950 °C. Interdigit Ni_2Si Schottky contacts, Ni stripes were fabricated on the wafer front side through an optimized thermal annealing process [2].
The fundamental aspect of these interdigit Schottky photodetectors is the direct exposure to radiation of the optically active area (*OAA*) that enable an improvement of the sensitivity at short wavelengths. The effects of material surface changes (thermal oxidation, ion-irradiation, etc.) on the UV-detector performances were also studied. In particular, a large photocurrent increase in 4*H*-SiC interdigit Schottky UV detectors was observed in the presence of a thermally grown silicon oxide layer, accompanied by long recovery times, due to the de-trapping of charges in the oxide after the UV-irradiation switching off [3]. The photoresponse of the device was analytically described considering the lowering of the surface potential barrier due to charges trapped at the oxide/semiconductor interface. Under ion-irradiation with 1, 4, and 10 MeV Si^+-ion beam, a change of the optical response of the detectors was observed, that in turn depended on the ion irradiation energy [4]. The optical effects were huge compared to the negligible variation of the reverse leakage current of the diodes under these irradiation conditions. This behavior was correlated to the nature of radiation damage.

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Elaboration and treatment of 3C-SiC heteroepilayers grown on silicon: from the material to GaN based applications

M. Portail[1,*], S. Roy[1], T. Chassagne[2], C. Moisson[2], Y. Cordier[1], E. Frayssinet[1] , M. Zielinski[2]
[1]*CNRS – CRHEA, Rue Bernard Grégory, 06560 Valbonne, France.*
[2]*NOVASiC, Savoie Technolac, Arche Bat 4, BP 267, 73375 Le Bourget du Lac, France.*
[*] Corresponding author: mpo@crhea.cnrs.fr

Many recent works and publications have put light on the interest of 3C-SiC epilayers grown on silicon as pseudo substrates for growth of gallium nitride and others III-N compounds. It is now well admitted that they constitute a promising alternative to silicon and hexagonal SiC substrates owing to the good balance between a reduced cost and good physical and chemical properties. But this interest is conditioned by the quality of the 3C-SiC material and the reduction of residual stresses within the 3C-SiC/Si epiwafer. A detailed structural analysis is thus required to better understand in what extent the lattice and thermal expansion coefficient mismatches as well as the process, used for the elaboration, generate extended defects and residual strain. As it is expected that the epilayer will remain very defective in comparison to "ideal" hexagonal bulk substrates, it is also important to investigate the effect of the post deposition processes as polishing and thermal annealing which can bring surface improvements very beneficial for GaN regrowth. Finally, it is of first importance to investigate the influence of a given structural property of the 3C-SiC epilayer on the GaN quality.

Here, we try to address some aspects of the above mentioned issues, namely (1) the influence of the conditions of deposition on the formation of extended defects, (2) the effect of the polishing and thermal annealing on the surface quality and (3) the influence of the 3C-SiC epilayers on the quality of GaN based structures.

In that work, 3C-SiC films were deposited on 2 and 4 inches (111) and (100) silicon substrates by means of resistively heated hot wall CVD, using propane and silane precursors. Some epiwafers were polished *via* CMP process using NOVASiC know how. Post deposition thermal annealing were realised at different temperatures (1100°C and 1300°C) under different ambient atmospheres (argon or hydrogen). Finally, GaN based structures were elaborated on differently treated 3C-SiC epilayers. A comparison with silicon substrate was also made. The GaN based structures were elaborated within MBE system using AlN buffer or AlN/GaN stress mitigating layers as nucleation step.

First, we have investigated the influence of the nucleation stage on the density of twin defects within (111) and (100) 3C-SiC films. A strong dependence with the propane flow rate is put in evidence as illustrated on figure 1. It is also demonstrated that the formation of twin defects is favoured within (100) films. The influence of the pre-process treatment is discussed: the introduction of a pre-annealing stage seems less favourable for the twin density but allows a reduction of the final film bow.

Secondly, we show the results of the CMP polishing process of (111) oriented 3C-SiC epiwafers. As illustrated on figure 2, a factor 10 reduction of the RMS roughness of the films can be obtained. The surface nevertheless still presents some typical defects attributed to the presence of stacking faults within the film. The annealing of the films (polished or not) induces some matter transport which is dependent on the nature of the gas. In case of argon treatment, the surface morphology reveals something typical of a step flow mode etching whereas in case of hydrogen annealing, the surface morphology is characterized by a step bunching type aspect. This is illustrated in figure 3. This effect is observed irrespectively of the polished character of the surface, but appears only after the 1300°C annealing.

Finally, some GaN based structures were grown on different type of surfaces, namely: (1) non polished 3C-SiC(111), (2) polished 3C-SiC(111) and (3) Si(111) surfaces. It was previously demonstrated that the electrical properties of the AlGaN/GaN HEMT developed on non polished 3C-SiC surfaces are at least equivalent to those obtained on silicon substrates (mobility more than 2050 cm²/Vs and carrier concentration more than 1x10+13cm² [1]). Here we present PL measurements which show how the use of 3C-SiC pseudo substrates allows obtaining a crack free GaN epilayer in a compressive mean state without using the stress mitigating layers. This is illustrated in figure 4.

This work is partly supported by OSEO Innovation in the framework of G2REC project.

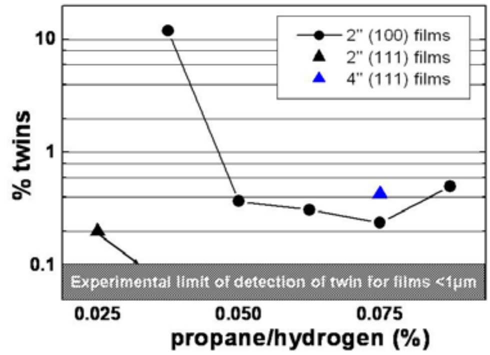

Fig.1: Evolution of the twin content within 3C-SiC epilayers grown on different substrates and for different propane dilution rates during the carbonization stage.

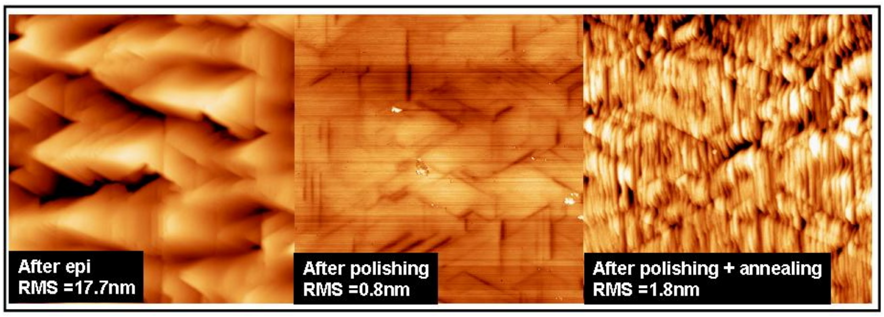

Fig.2: Evolution of the surface morphology of 3C-SiC epilayer grown on 2'' 4°off silicon substrate.

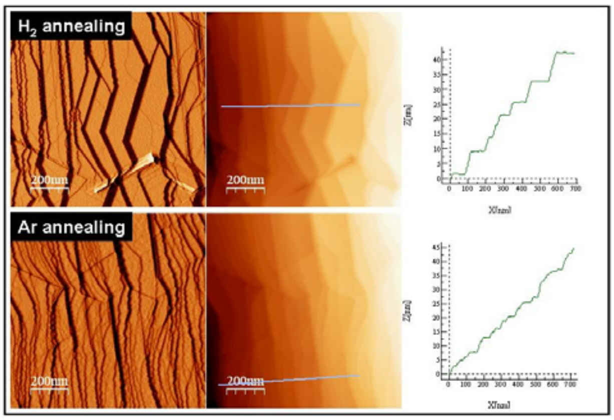

Fig.3: Effect of the thermal annealing performed on 4°off 3C-SiC(111) epilayer.

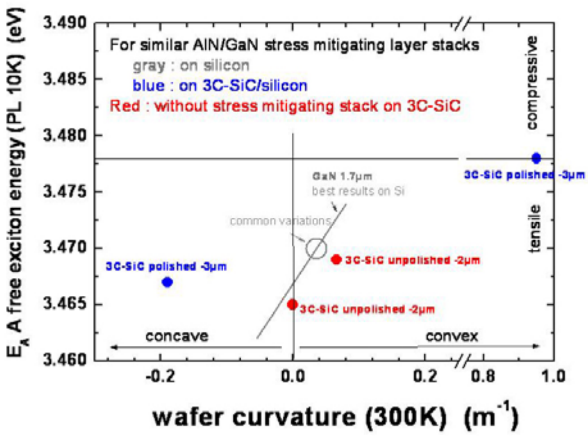

Fig.4: Comparison of the residual strain measured by PL obtained on GaN films grown on 3C-SiC(111) epilayers

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3C-SiC growth on off-axis Si substrates

A. Severino[1*], M. Camarda[1], G. Condorelli[2], M. Mauceri[2], N. Piluso[1], R. Anzalone[1], B. Cafra[3], M.A. Di Stefano[3], A. La Magna[1], G. Abbondanza[2], F. La Via[1]
[1]*CNR-IMM, Strada VIII, n.5, Zona Industriale, 95121 Catania, Italy*
[2]*Epitaxial Techn. Center, 16ª Strada, Contrada Torre Allegra, 95030, Catania, Italy*
[3] *ST-Microelectronics, Stradale Primosole 50, 95121 Catania, Italy*
[*]Corresponding author: andrea.severino@imm.cnr.it

3C-SiC heteroepitaxy on Si is usually characterized by a large amount of structural defects due to very high lattice parameter (~20%) and expansion coefficient (~8%) mismatches. The heteroepitaxial growth of several semiconductors using Si as substrate has been advancing rapidly and the use of off-axis substrates has been a contributing factor. [1]
3C-SiC film growth was performed in a hot-wall chemical vapor deposition (CVD) reactor. After a 10 minute carbonization step at 1120 °C in an hydrocarbon ambient with ethylene as carbon precursor. No gas were introduced during the heating up from carbonization to the growth temperature. Trichlorosilane (TCS) and ethylene were then used as growth precursors at 1380 °C (T_g) with a constant C/Si ratio of 1.2. Different growth runs were performed to obtain a 3C-SiC film thickness ranges between 2 µm and 12 µm with a growth rate of about 6.5 µm/hr. X-ray diffraction (XRD), transmission electron microscopy (TEM), atomic force microscopy (AFM) and curvature radius calculations have been employed as techniques to investigate 3C-SiC structural properties.
In figure 1a the average residual stress of the system is plotted with the 3C-SiC film thickness as measured from the modified Stoney equation. [2] This plot shows that the average residual stress in the heteroepitaxial system is doubled when the growth is performed on an off-axis substrate towards the [112] as compared with films grown on substrate off-axis along the [110]. As can be seen, the measured stress in the film decreases with the increasing of the 3C-SiC film thickness probably due to crack formation, as seen under optical microscope investigation and reported by others by a low temperature growth process experiment. It is worthy to note that after a few microns of growth the whole wafer shows a bow around a direction as an effect of the mismatches. The bow we found in this set of experiment was along a defined axis as expected if you are dealing with off-axis substrates as found out recently also for 3C-SiC growth on off-axis (100) Si. [3-4] In fact, the off-angle cut breaks the rotation symmetry of the (111) Si surface setting two non-equivalent directions, one parallel to the cut and another one orthogonal to it, thus, for symmetry reasons, the stress axis will belong to one of the two. This is confirmed by profile analysis performed with a VEECO optical profilometer, as reported in figure 2a where it is shown a 3-D image of a 6 µm 3C-SiC sample. Such a kind of measurements allows us to calculate precisely the curvature radius along all of the direction required. Figure 2b shown two line profiles along perpendicular directions onto the surface. The variation in Δz between the two directions is considerable and the asymmetry is easily deduced.
The formation of several crystalline defects has been seen as the most effective way to relieve the strain induced by mismatches between the two dissimilar materials. [5] Stacking fault (SF) generation is also involved in this relaxation mechanism. In our study, SF density is doubled for growth on substrates with a miscut towards [112] as compared with [110]. On the other hand, since the bow is higher when the growth is performed on a miscut along [112] as well as the residual stress, we were expecting to find a lower SF density on such a heteroepitaxy. The trend in stacking fault density, reported in figure 1b, can be related to a different surface morphology detected on the different sets of samples suggesting, as will be shown, a tight relation between stacking fault generation and propagation, stress relaxation and surface morphology observed after the growth. [6] A further study has been conducted on off-axis

(100) Si and (111) Si substrates, with the miscut axis along the [110]. Raman microscopy has been used to evaluate the residual stress and defects by considering the full width at half maximum (FWHM) of the transversal optical phonon mode vibrations, as shown in figure 3. XRD FWHMs of epitaxial 3C-SiC peaks show a decreasing trend suggesting an improvement in the crystal quality of overgrown 3C-SiC film while, on the other hand, Raman TO FWHMs follow the same trend for (111) Si and an opposite one for (100) Si. By this comparison, another mechanism of stress relaxation, beyond to the crystal defect generation, seems to be involved in (100) 3C-SiC.

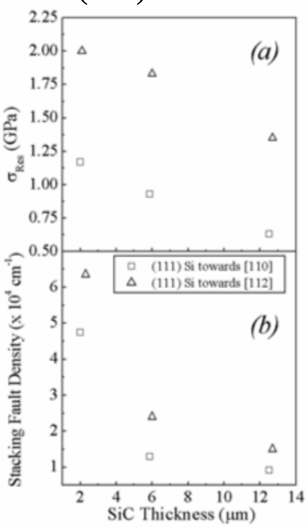

Fig. 1: *(a)* Average residual stress and *(b)* stacking fault density of 3C-SiC films grown on (111) Si with off-cut axis towards [110] and towards [112].

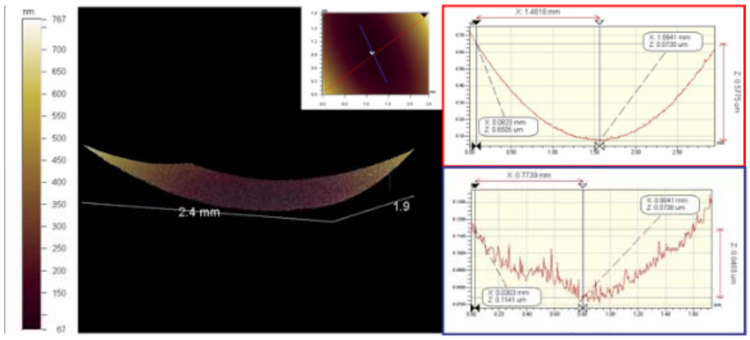

Fig. 2: 3-D picture of a 6μm thick 3C-SiC film on off-axis (111) Si. On the right there are shown line profile of the wafer along two different directions, the red along the curvature and the blue along the curvature axis.

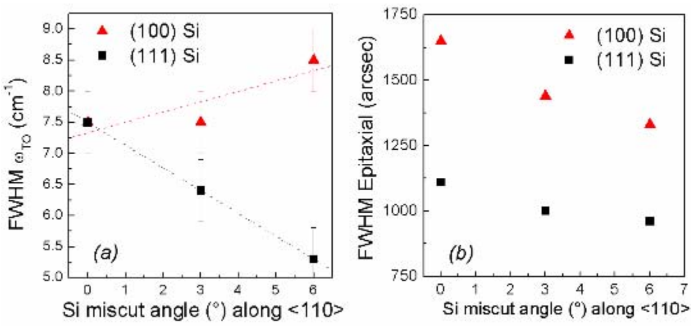

Fig. 3: FWHM trends of Raman TO 3C-SiC phonon mode and of epitaxial 3C-SiC XRD peak. Sample thickness is about 3 μm.

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TEM analysis of twins and interfacial defects in 3C-SiC grown on Si (111) by CVD

S. Roy [1*], M. Portail [1], T. Chassagne [2], J. M. Chauveau [1], P. Vennéguès [1] and M. Zielinski [2]
[1]*CNRS – CRHEA, Rue Bernard Grégory, 06560 Valbonne, France.*
[2]*NOVASiC, Savoie Technolac, Arche Bat 4, BP 267, 73375 Le Bourget du Lac Cedex, France.*
* Corresponding author: sebastien.roy@crhea.cnrs.fr

In this work, the influence of the carbonization conditions on the formation of crystal defects in 3C-SiC layers is investigated by cross-sectional and plan view Transmission Electron Microscope (TEM) analyses. The 3C-SiC films are grown on (111) oriented, on axis, silicon substrates in a horizontal resistively heated CVD reactor [1] using propane and silane precursors. We used the classical two-step process, proposed by Nishino et al. [2], including the carbonization at 1100°C under a mixture of propane and hydrogen and the growth at a temperature of 1350°C under silane, propane and hydrogen.

Previous works [3,4] have shown the importance of the carbonization step on the final crystalline quality of SiC films. More specifically, it has been demonstrated that a low propane flow rate induces a poor nucleation density and hence highly defective layers with coalescence defects, a high roughness and a high density of voids below the interface. At the opposite, the samples elaborated with higher propane flow rate exhibit a smooth surface, a very low density of voids and no macroscopic defects are observed. TEM analyses were performed on samples elaborated with low and high propane flow rate, corresponding respectively to a dilution of 0.028 % and 0.043 % in hydrogen. The cross section specimens were prepared along the (1-10) plane. They were mechanically thinned and polished and the electron transparency was obtained using Ar ion milling.

We first observe, on each sample, a high density of stacking faults (SFs) and planar microtwins along the (-1-11) planes (fig. 1). The high resolution picture of fig. 1a shows that the microtwins consist in a 180° rotation of the crystal around the [-1-11] axis. The microtwins and the SFs create typical lines on the diffraction pattern as shown in fig. 1c. The linear density of SFs and twins is found to be independent on the propane flow rate and is estimated at $4\text{x}10^5$ cm^{-1} (on bright field pictures). Due to the (111) orientation of the growth, these planar defects cannot eliminate by mutual interaction as in the case of the (100) oriented epitaxy, and then they propagate through the whole thickness of the film.

The TEM observations also revealed another kind of defects which are basal twins (fig. 2). The basal twins are specific to the (111) oriented epitaxy of SiC and consist in a 180° rotation of the SiC crystal around the [111] growth axis (they are also called double positioning domains). They create additional diffracted spots on the diffraction pattern as shown on fig. 2c. One of these spots was used for the dark field micrographs presented in fig. 2a and 2b. The basal twins are formed during the first stage of the nucleation and their size and density are then strongly dependent on the carbonization conditions: for the samples elaborated with high propane flow rate, the basal twins are small (60 to 80 nm width) and a lot of basal SFs and microtwins are confined in a 25 nm layer close to the interface (fig. 2a). For the samples grown with low propane flow rate, the basal twins are much bigger (300 to 400 nm width) as shown in fig. 2b and some of them may reach the layer surface. The huge size of the basal twins is attributed to the poor nucleation site density which induces a high nuclei size and hence the 3D growth of large islands during the buffer formation. The X-ray diffraction analyses confirm the differences between the samples: on the samples with low propane flow rate, a set of diffraction peak shifted at 60° is observed on the azimuthal scans recorded along the asymmetric {113} direction (fig. 2d) traducing the presence of basal twins. These peaks are not observed on the samples with higher propane flow rate because of the smaller volume ratio between twinned and un-twinned areas.

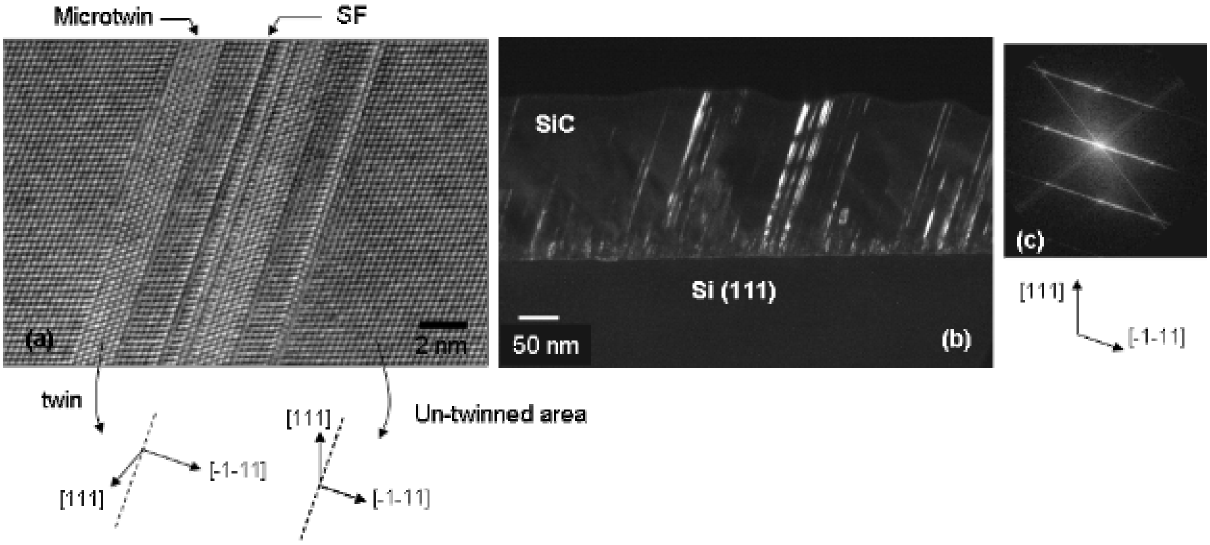

Fig.1: (a) High resolution micrograph of stacking faults and microtwins along (-1-11) planes. (b) Dark field imaging of the planar defects. (c) Diffraction pattern along the [1-10] zone axis with diffraction lines due to SFs.

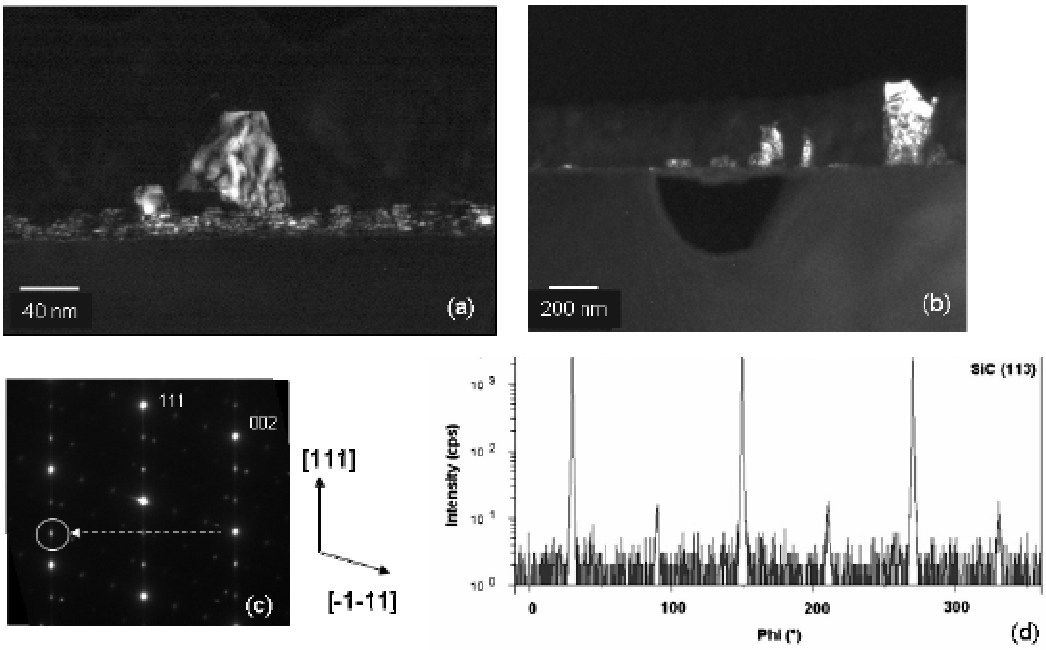

Fig.2: (a) Dark field imaging of a small basal twin (65 nm width) in a sample elaborated with high propane flow rate during carbonization. (b) Dark field imaging of large basal twins (300 nm width) in a sample elaborated with low propane flow rate. (c) Diffraction pattern with projected spots due to the basal twinning. (d) Azimuthal XRD scan recorded along the asymmetric {113} direction on the sample with low propane flow rate.

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Epitaxial Growth of 3C-SiC on AlN/Si (100) via Methyltrichlorosilane-based Chemical Vapor Deposition

Wei-Cheng Lien[1*], Kan Bun Cheng[2], Debbie Senesky[2], Carlo Carraro[1], Albert P. Pisano[2], Roya Maboudian[1]

[1]*Department of Chemical Engineering, University of California, Berkeley, 94720 California, USA*

[2]*Department of Mechanical Engineering, University of California, Berkeley, 94720 California, USA*

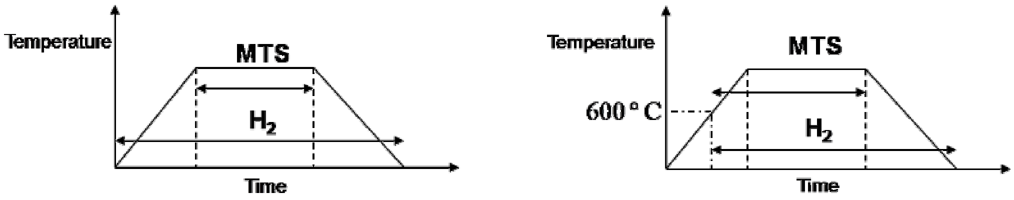
[*] Corresponding author: wclien@berkeley.edu

Silicon carbide (SiC) is a semiconductor material that is emerging as an alternative to silicon-based high-power electronic circuits [1]. The wide band-gap (2.3 eV), high breakdown field (3 MV/cm), high saturated electron velocity (2.5×10^7 cm/s) and high thermal conductivity (5 W/cm-^{o}C) of 3C-SiC supports the use of this material for high-power electronics [2]. The interest in thin film growth of high quality SiC on aluminum nitride (AlN) dielectric is due to the importance of semiconductor-on-insulator structures, in which insulating layer provides high-quality electrical isolation under harsh environment. Excellent thermal stability and close thermal expansion coefficient with SiC make AlN an excellent choice as the dielectric layer [3].

Heteroepitaxial AlN films are grown on Si (100) at 350 ˚C with Tegal AMS SMT reactive sputtering system. The FWHM of XRD rocking curve of AlN (0002) is 1.3˚, suggesting a high degree of crystallinity. SiC deposition is performed inside a hot-wall LPCVD reactor (Thermo Electron Corporation, Lindberg/BlueM, HTF55122A). SiC films are grown using single-source precursor methyltrichlorosilane (MTS, CH_3SiCl_3, 99%) and high-purity hydrogen (99.9% +) is used as a carrier gas. Two different precursor feeding procedures are employed (Fig. 1). For the feeding procedure I the reactor temperature is raised to 1200 ˚C in a flow of H_2 (70 sccm) then the MTS (0.7 sccm) is introduced. For the feeding procedure II, the substrate is initially heated up to 600 ˚C, and then MTS (0.7 sccm) and hydrogen gas (70 sccm) are introduced simultaneously, then the temperature is further raised to 1200 ˚C with heating rate of approximately 1.5 ˚C/sec. During growth, the reactor pressure is maintained at around 1.10 Torr. At the end of the deposition, the reactor is cooled down to room temperature under hydrogen gas flow at a cooling rate of 0.2 ˚C/sec.

Fig. 2 shows the Raman spectra of an AlN/Si (100) substrate, and of a series of SiC films on AlN/Si (100) obtained by different feeding procedures. The presence of Raman peaks of AlN at planar E2 symmetry 247.8 cm^{-1} (low mode), axial A1 symmetry 618.5 cm^{-1} (TO mode), planar E2 symmetry 656.9 cm^{-1} (high mode), and axial A1 symmetry 888.4 cm^{-1} (LO mode) indicate the AlN films have been deposited on Si (100). SiC films grown by procedure II exhibit a sharper Raman transverse optical (TO) SiC peak at 794.6 cm^{-1} and longitudinal optical (LO) SiC peak at 968.2 cm^{-1} than the films using procedure I. Due to poor acid resistance of AlN, it is known byproduct hydrochloride gas at 1200 ˚C readily etches AlN and roughen the surface; therefore the SiC films using feeding procedure I exhibits low degree of crystallinity as shown in Fig. 3(a). However, films using procedure II have deposited about 100 nm buffer SiC layer between AlN and the epitaxial film at lower temperature to protect the AlN being attacked by HCl; therefore heteroepitaxy of 3C-SiC/AlN/Si (100) are achieved (Fig. 3 (b)).

In conclusion, methods of depositing 3C-SiC/AlN/Si (100) have been demonstrated, paving the way for SOI structures as well as MEMS application.



(a) (b)

Fig. 1. Two different precursor feeding procedures: (a) procedure I, (b) procedure II.

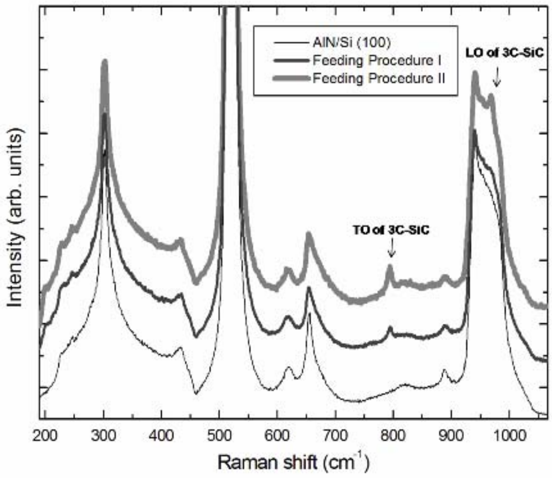
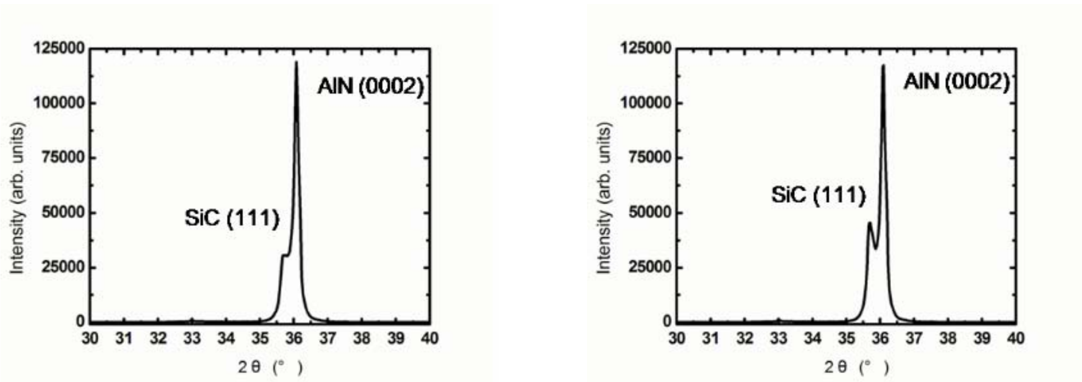


Fig. 2. Raman spectra of an AlN/Si (100) substrate, and of a series of SiC films on AlN/Si (100) obtained by different feeding procedures deposited at 1200 ˚C and H_2/MTS flow rate ratio at 100.



(a) (b)

Fig. 3. XRD spectra of 3C-SiC films using (a) procedure I and (b) procedure II (synthesis temperature: 1200 ˚C, H_2/MTS flow rate ratio at 100).

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Growth and characterization of 3C-SiC grown using CBr_4 as a precursor

G.Attolini[1], M.Bosi[1], F.Rossi[1], B.E. Watts[1*], B. Pécz[2], L. Dobos[2] and G. Battistig[2]
[1]*IMEM-CNR Institute Parco Area delle Scienze 37 A, 43010 Parma (Italy)*
[2]*Research Institute for Technical Physics and Materials Science, Hungarian Academy of Sciences, P.O. Box 49, H-1525 Budapest, Hungary*
[*] Corresponding author: watts@imem.cnr.it

The growth of SiC on Si is being studied for many diverse applications and so the search for precursors that could be used to grow with improved or novel physical, structural and morphological properties is a relevant issue in this field. Here we present a study of the use of CBr_4 as a precursor in the deposition of 3C-SiC in a cold walled MOVPE reactor.
The growth has been studied in a range of temperatures between 1100 and 1250 °C, on differently oriented substrates.
XRD spectra of the layers show a single peak at 41.5°, ascribed to the 200 β-SiC reflection., texturing confirmed by TEM cross-sectional images of films grown at 1200°C and 1250°C shown in Fig. 1. Previous works using carbon and silicon tetrachlorides produced only polycrystalline, untextured films [1, 2]. The quality of the Si/SiC interface is worth noting: as the boundary between the film and Si is sharp and defects in the substrate are absent. Furthermore, there are few crystalline defects in the SiC itself, only some stacking faults along the (111) crystalline planes were observed.
SEM images, obtained on samples grown at 1200°C and below indicate the presence of microcrystals on the surface (Fig.2), which are prismatic with well developed facets. The facets were further studied by AFM. The square pyramid in Fig. 3 shows hillocks about 0.8 μm high and 1.5-2 μm at the base. There is some variability in the shape of the pyramids growing on (001) Si that depends on the temperature and location on the wafer. However, this family of facets that are typically seen on all the (001) oriented films. Here four facets tilted towards (110) from the (001) normal direction are well developed and the analysis indicates that they are tilted about 23-27° from the (001) direction, close to the calculated value of 25.2° of a {311} plane. Faceting of the hillocks on (111) Si showed all the family of {311} planes. These could be indexed with greater confidence as the facet inclination was very close to the theoretical value of 29.5° calculated for the (311) $\angle$ (111) interplanar angle.
In GaAs/Si growth Usui et al [3] found crystals with a similar growth habit to those observed, growing first as rounded domes and then developing {311} and {111} facets. Thus, {311} planes seem to be the stable facets for the S-K type growth of compounds having the zinc blende structure. Carbon contamination is known to lead to faceting on the surface of nominally pure silicon of pits when Si is sublimed from the surface [4].
There are other phenomena that must also be considered. The <311> axes are polar, so C and Si planes may have different stabilities. Jacobi et al [5] observed that the pitting behaviour could result in a pit surface or a two surfaces, having indices (214) and (124). Vetter and Dudley [6] studied 3C-SiC crystals grown using the Baikov technique. In this case, {211} and {100} facets grow. Clearly, faceting depends on growth conditions such as temperature but most importantly C:Si ratio.
Clearly, faceting in SiC is difficult to interpret because of several concurrent factors taking place during the growth (precursor decomposition rates, precursor concentrations) but the high index {311} planes are worthy of study for growth purposes to see if a greater degree of smoothness can be obtained on epitaxial films.
In conclusion, oriented well crystallised SiC grown on Si using CBr_4. Defects, namely voids, wormholes, or interfacial roughening were not observed at the SiC/silicon interface. These experiments demonstrate that it is possible to grow well crystallised and oriented 3C-SiC using carbon tetrabromide Well-developed facets are observed under particular conditions, a

feature that is seen commonly when using halogenous precursors. SiC grows epitaxially even at 1000 °C but the growth mode is 3D island rather than 2D planar. Stable facets appear to be {111} and {113} planes for films grown on both 111 and 001 silicon substrates.

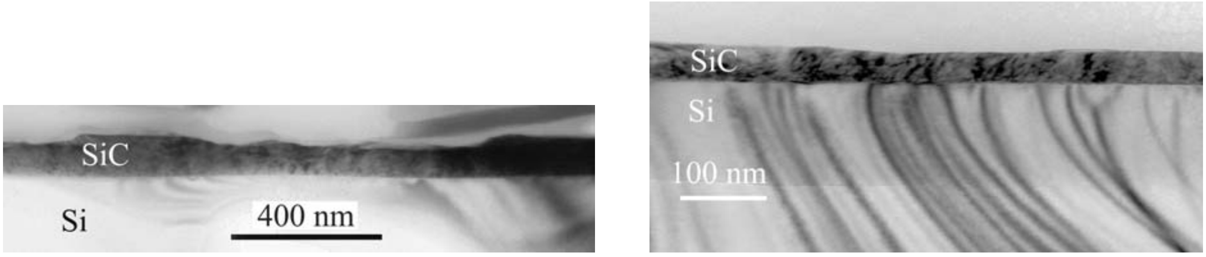

Fig. 1: TEM images of SiC sample grown at 1200°C (left) and 1250 °C (right)

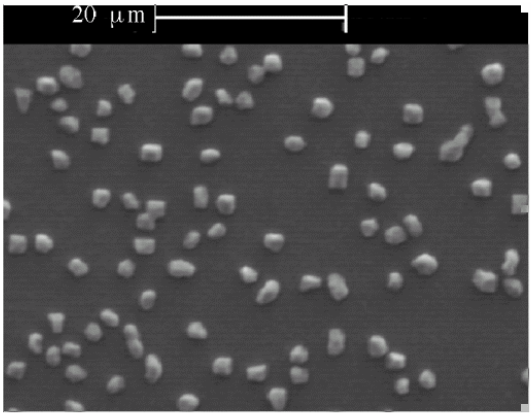

Fig.2: SEM image of SiC grown at 1200°, showing hillocks

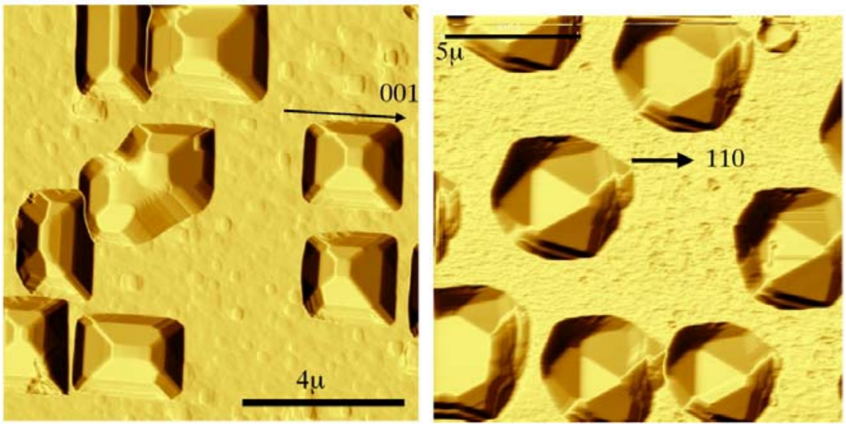

Fig.3: AFM images of SiC surface grown at 1200 on Si 001 (left) and Si (111) right

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Growth of cubic GaN and AlGaN/GaN on 3C-SiC

D.J. As*
University of Paderborn, Warburger Strasse 100, 33098 Paderborn, Germany
* Corresponding author: d.as@uni-paderborn.de

Commercially available group III-nitride-based electronic and optoelectronic devices are grown along the polar c direction, which suffer from the existence of strong “built-in” piezoelectric and spontaneous polarization. This inherent polarization limits the performance of optoelectronic devices containing quantum well or quantum dot active regions. To get rid of this problem much attention has been focused on the growth of non- or semi-polar (Al,Ga,In)N in the last years. However, a direct way to eliminate polarization effects is the growth of non-polar (100) oriented zinc-blend III-nitride layers. With cubic epilayers a direct transfer of the existing GaAs technology to cubic III-Nitrides will be possible and the fabrication of divers electronic and optoelectronic devices will be facilitated. However, since cubic GaN is metastable and no cubic GaN bulk material exists in nature, heteroepitaxy with all its drawbacks due to lattice mismatch is necessary to grow this material. Due to the low lattice mismatch to cubic GaN the substrate of choice for the growth of cubic III-nitrides is 3C-SiC.

In this talk the latest achievements in the molecular beam epitaxy of phase-pure cubic GaN, AlN and their alloys grown on 3C-SiC substrates is reviewed. A new RHEED control technique [1] is presented to carefully adjust stoichiometry and to severely reduce the surface roughness, which is important for any hetero-interface. The structural properties measured by high resolution X-ray diffraction are shown in Fig. 1 for GaN epilayers with different layer thickness and surface roughnesses. The absence of polarization fields in cubic nitrides is demonstrated [2] and in Fig. 2 near 1.55µm inter-subband absorption in cubic AlN/GaN superlattices is shown [3, 4]. Figure 3 depicts the electrical properties of Ni-Schottky-barrier devices [5] on cubic GaN and shows the influence of thermal treatments and rapid thermal annealing (RTA) on the I-V characteristics. The progress towards the fabrication of C-doped insulating cubic GaN buffer layers is outlined [6] and the development of cubic Hetero-FETs is discussed. In Fig. 4 the room temperature output characteristics (I_{DS}-V_{DS}) of cubic AlGaN/GaN HFET is presented after subtraction of the c-GaN buffer conductivity[7].

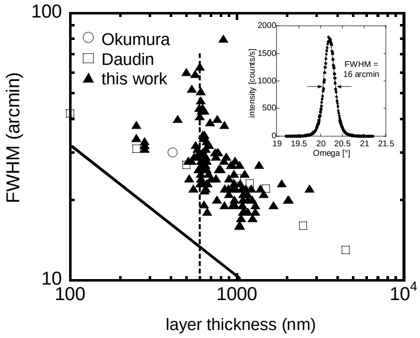

Fig. 1: Rocking curve linewidth of cubic GaN epilayers grown on 3C-SiC substrates versus thickness of the cubic epilayers.

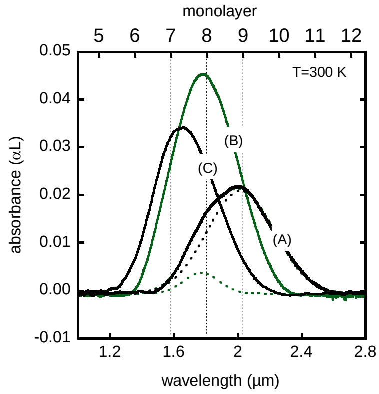

Fig. 2: Optical absorption spectra of the intersubband transitions in cubic GaN/AlN short period multible quantum wells (MQWs).

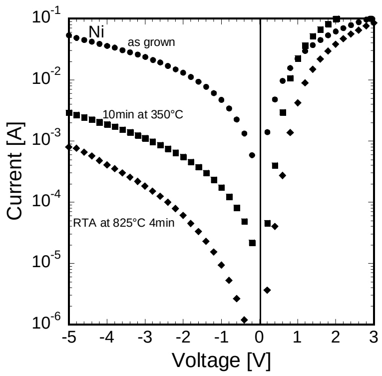

Fig. 3: Room temperature current voltage (I-V) characteristics of a Ni-Schottky contact on cubic GaN before annealing (full circles), after annealing in air at 350°C (full squares and after RTA at 25°C (full diamonds).

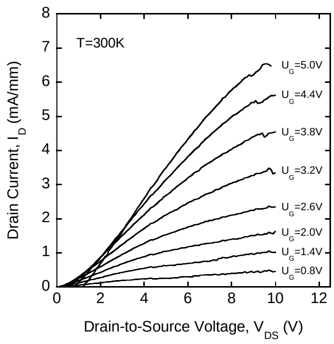

Fig. 3: I_{DS}-V_{DS} characteristics of a cubic AlGaN/GaN HFET measured at room temperature after subtraction of the c-GaN buffer conductivity.

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3C-SiC Epitaxial Layer grown on Si (001) and Si (001) 4° off-axis Substrates

G. Wagner[1*], J. Schwarzkopf[1], M. Schmidbauer[1], M. Luysberg[2] and R. Fornari[1]
[1]*Institut für Kristallzüchtung, Max-Born-Str. 2, D-12489 Berlin, Germany*
[2]*Forschungszentrum Jülich, Ernst-Ruska-Zentrum, D-52425 Jülich, Germany*
[*] Corresponding author: wagner@ikz-berlin.de

The advantages of using silicon as a substrate in heteroepitaxy of 3C-SiC are the large size, high quality, low price and good polytype control. Due to the large lattice mismatch and the difference in thermal expansion coefficient between Si and SiC a significant density of planar defects are generated in the 3C-SiC layers. The most common defects in the 3C-SiC layers are stacking faults (SFs), twins (Ts) and anti-phase boundaries (APBs). APBs can be eliminated by growing 3C-SiC on misoriented Si(001) however SFs remain unaffected [1]. The stacking faults density can be reduced by acting on the carbon-silicon ratio as well as carbon and silicon to atomic hydrogen flux ratio at the surface during carbonisation and layer deposition [2].

The purpose of this study is to compare the influence of the Si(001) substrate orientation on defect generation and the incorporation of alumina in 3C-SiC layers. Single-crystalline 3C-SiC epitaxial layers were grown on two-inch on-axis Si(001) (type1) and 4° off-axis Si(001) substrates (type 2) by low-pressure hot-wall chemical vapour deposition. Silane and propane diluted in hydrogen were used as precursors. The 3C-SiC layers on both types of substrates were investigated by means of x-ray diffraction (XRD), atomic force microscopy (AFM), high-resolution transmission electron microscopy (HR-TEM) and secondary ion mass spectroscopy (SIMS).

The 3C-SiC layers were deposited, at a deposition temperature of 1350° C, immediately after the carbonization of the surface of the Si-substrates using propane and a small amount of silane at temperatures between 800°C and 1350°C. The management of Si-partial pressure in the gas atmosphere inhibited the appearance of voids or inclusions at the interface between the substrate and layer. Growth on on-axis oriented Si(001) substrates is characterized by the formation of high density, of three-dimensional domains with grain size increasing with increasing layer thickness. The surface shows a mosaic pattern that arises where the horizontal and vertical anti-phase domains cross at right angles. (fig.1a). The crystal orientation of adjoining APDs is equivalent, except for those rotated 90° around the [001] axis. On the other hand the growth on 4° off-axis Si substrates shows a step flow growth mode. Figure 1b shows the surface of 3C-SiC grown on Si(001) 4° of-axis in [001] direction. In contrast to figure 1a the step edges of the layer are oriented in [001] direction. XRD-investigation has shown that the full width at half maximum (FWHM) of the rocking curve decreases from about 600 arcsec to about 300 arcsec when layer thickness increases from 5 µm to 18 µm. Figure 2 shows that the FWHM value of layers type1 is about 20% larger than the width of the rocking curve of type 2 layers at comparable layer thicknesses. It implies a lower defect density in type 2 layers, particularly with regard to the disappearance of anti-phase domain boundaries. However, a comparison of HR-TEM images shows no remarkable differences in the density of misfit dislocations at the interface and stacking-faults in the grown layers. AFM measurements have shown that the surface roughness of type1 layers is larger in comparison to that of type 2 layers. The layer roughness increases with increasing layer thickness and domain size (type1) whereas the roughness on type 2 layers seems to be independent of the layer thickness (fig 3). This effect is also related to the disappearance of anti-phase domain boundaries in layers of type 2 and the different growth modes. The Al-concentration in Al-doped 3C-SiC layers, determined by SIMS measurements, are in layers of type-2 about two times higher than in layers of type1 grown under the same gas flow conditions and at equal deposition temperature (fig. 4). Considering that the aluminum atoms occupy the Si-position in SiC lattice, these observations may be explained by the polarity of the step edges present in off-oriented material. It was indeed found that the step edges was always present the Si-face when Si substrates off-oriented towards [001] are used.

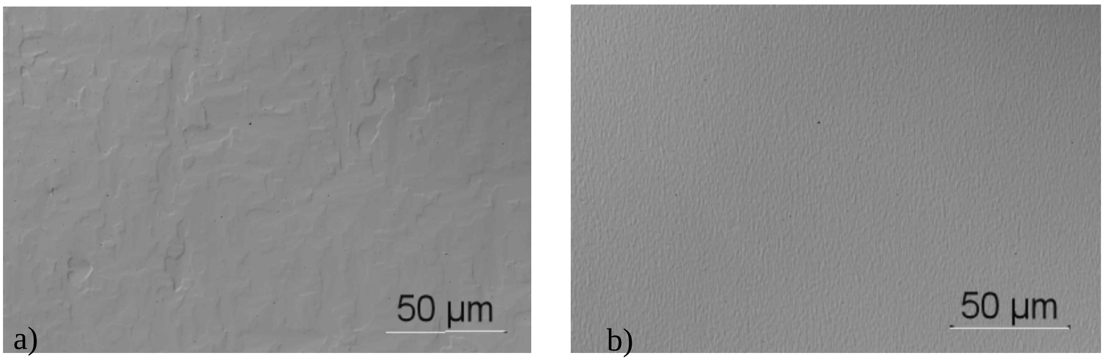

Fig. 1: Optical microscope image of a 3C-SiC surface grown on Si(001) substrate on-axis (a) and on Si(001) substrate 4° off-axis towards [001] direction (b).

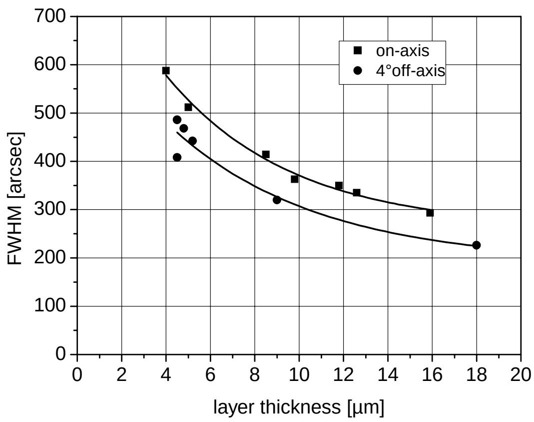

Fig. 2: FWHM of the rocking curve in dependence on the epitaxial layer thickness and substrate orientation

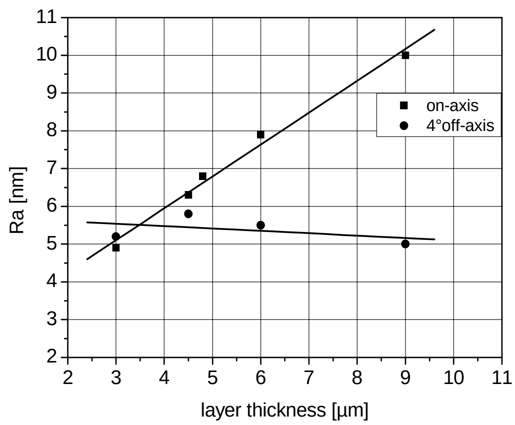

Fig. 3: Surface roughness Ra of 3C-SiC layers in dependence on layer thickness of on-axis and off-axis Si(001) substrates.

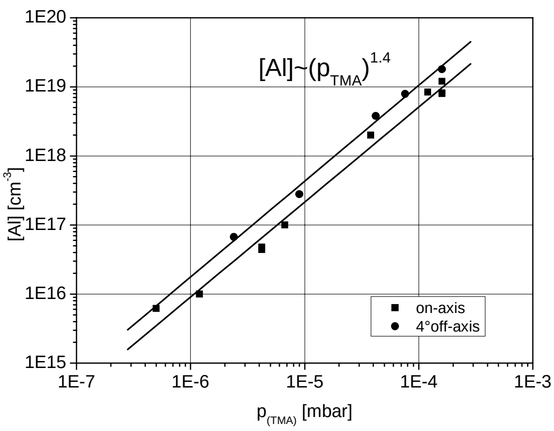

Fig. 4: Aluminum concentration (SIMS) in dependence on the Trimethylaluminium –partial pressure in 3C-SiC layers on Si(001) on-axis and 4° off-axis

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Numerical study of the evolution of substrate defects during the growth of epitaxial SiC films

M. Camarda[1*], A. La Magna[1], F. La Via[1]
[1] *Consiglio Nazionale delle Ricerche - Istituto per la Microelettronica e Microsistemi*
Strada VIII n. 5, Zona Industriale, I- 95121, Catania, Italy
[*] Corresponding author: massimo.camarda@imm.cnr.it

Epitaxial growth is a commonly used technique to produce high quality monocrystalline semiconductor layers required for electronic devices. In this growth method, the use of substrates exposing vicinal surfaces, which generates a sequence of parallel steps on the crystal surface, can help in preventing island nucleation and, thus, reducing the surface roughness. This technique is called "step-controlled epitaxial growth" or step flow, and it allows also, when close packed structures are processed (i.e. in the case of many compound semiconductors such as SiC, GaN, GaAs etc) to hinder the generation of stacking faults, basal plane dislocations and polytype inclusions.

In the past, the step flow growth was studied applying either continuous models[1], atomistic simulations[2,3,4], or both in a hybrid continuous-atomistic schema[5]. All these approaches consider an ideal substrate with a surface made of a sequence of straight steps separated by terraces of widths $l=h/\tan\alpha$, being α the misorientation cut and h the step height, and are aimed to estimate a critical growth rate, Gr_{lim} (a critical temperature T_{lim}), above (below) which 2 dimensional island nucleation occurs.

In the past this growth process was studied starting from ideal substrates (i.e. defect free substrates), thus, considering the problem of defect generation rather than defect propagation. Whereas, even well within the step flow regime, the quality of the grown crystal can be strongly affected by the propagation of the defects from the substrate into the epilayer [6,7].

In order to study this problem we have used an atomistic, kinetic Monte Carlo simulations on superlattice which consider, within the perfect crystal structure, defective sites identified as complementary sites for each (0001) hexagonal close packed (hcp) layer (or, equivalently, for each (111) layer in the case of cubic diamond or Zincblende structures). We started, in contrast with previous calculations[1-5], with a defective substrate containing a dislocation on a single, basal plane, layer with a Burgers vector equal to 1/3[10-10] (i.e. parallel to the step flow). In the Zhdanov's notation this defect corresponds to a (+2,-2) → (+1,-1,+1,-1) transformation. We have, then, studied the evolution of this defect, varying the growth rate of the process. We obtain the unexpected result that high growth rates (i.e. out-of-equilibrium deposition conditions) can hinder the propagation of the defect and thus lead to higher quality films. We hereby note that the range of explored growth rates is below the step-flow to 2D island transition, above that value (i.e. above Gr_{lim}) new defects will nucleate into the epitaxial film (i.e. there will be "in-grown" defects) and the usual dependency between the crystal quality and the growth rate will be restored. This unexpected behavior can be explained in terms of a kinetic competition between the expansion of the defect and that of the perfect crystal on the specific exposed, free, surface. Specifically, if the kinetic of the defect is higher with respect to that of the surrounding steps (which have the symmetry of the perfect, defect-free, crystal) the defect will tend to expand during the growth, in the opposite case it will shrink and, for long thick enough epilayers, it will close into a dislocation loop. The ratio between the lateral effective velocity of the defect and the lateral velocity of the step ($R=v_{defect}/v_{step}$) specifies the evolution of the defect during the growth. In general, R depends both on the crystallographic structure of the exposed surface and on the deposition conditions. In order to better describe the properties of the defect, we can define an "order parameter" $\theta=(Gr_{lim}-Gr)/Gr_{lim}$ (i.e. θ specifies the distance from the step-flow to 2D island nucleation transition) and obtain the following important phenomenological result: $\delta L_{def}/\delta\theta>0$. This

relationship is particularly important because it allows to determine, on the basis of the $Gr_{lim}(\alpha)$ and $Gr_{lim}(T)$ dependencies, the lateral extension of the defect (L_{def}) varying the misorientation cut (α) or the growth temperature (T).
Specifically, for the particular extended defect considered, in the case of the epitaxial growth of 4H misoriented towards the <11-20> direction[8], L_{def} is found to be an increasing function of the misorientation cut and an increasing function of the temperature. The dependency of L_{def} on the growth rate has been experimentally confirmed in [6,9], whereas, in [10] has been proven that the use of a low misorientation cuts (α=4°) can help in closing the basal plane dislocations. Finally, the dependency of L_{def} on the temperature has never been experimentally tested. Simulations are underway to extended this study to other basal plane defects and other substrates polytypes.

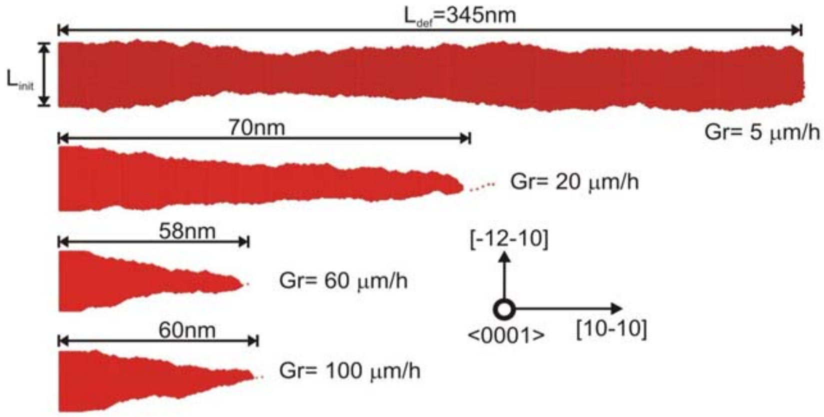

Fig.1: Plan view of the grown (1,-1,+1,-1) defects for different growth rate . We note that, at the slowest growth rate of Gr=5 μm/h the defect never closes, i.e. the defect length L_{def} exceeds the computational box. The initial extension of the defect along the [-12-10] direction (L_{init}) is the same for all the simulations. It is the equivalent of the panchromatic cathodoluminescence experimental images (see, for example Fig.1 of [11])

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Comparison of 3C-SiC Films Grown on Si(001) and Si(111)via Hot-wall CVD

C. Locke[1,*], R. Anzalone [2,3], A. Severino [2], C. Bongiorno [2], F. La Via [2], S. E. Saddow [1]

[1] *Electrical Engineering Dept., University of South Florida, 4202 E. Fowler Ave., Tampa, FL, 33620, USA*

[2] *CNR-IMM, Strada VIII, n.5, Zona Industriale, 95121, Catania, Italy*

[3] *University of Catania, Phys. Dept., via Santa Sofia 64, 95125, Catania, Italy*

[*] Corresponding author: aclocke@mail.usf.edu

The growth of 3C-SiC on Si substrates offers the prospect of a low cost, high performance semiconductor film for advanced electronic and mechanical devices and sensors. Unfortunately, the as-grown 3C-SiC films on Si films suffer from a large amount of defects caused be the 20% lattice mismatch and 8% coefficient of thermal expansion disparity between Si and 3C-SiC which results in a rough mesa-like growth structure [2]. In particular the surface morphology of 3C-SiC grown on (001) oriented Si is highly irregular thus making device processing difficult.
Fortunately, growth on (111) oriented Si results in a much smoother morphology with nearly flat surface topology and reduced micro-twin formation. Comparison of the X-ray diffraction rocking curve full-width half-maximum (FWHM) of the 3C-SiC(111) and 3C-SiC(200) peaks show similar crystal quality between the films grown on the two substrate orientations. Based on X-ray polar figure mapping, it was observed that the micro twin content for 3C-SiC grown on Si(111) was below the detection limit of the technique while the 3C-SiC grown on Si(100) indicated micro-twin formation in the <111> direction. X-TEM, SEM, and AFM characterization was also performed on the 3C-SiC films grown on the two orientations and will be presented.

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Very large monolayer graphene ribbons grown on SiC

N. Camara[1*], G. Rius[1], J-R. Huntzinger[3], A. Tiberj[3], N. Mestres[2], F. Pérez Murano[1], P. Godignon[1] and J. Camassel[3]

[1] *IMB-CNM-CSIC, Campus UAB, 08193-Bellaterra, Barcelona, Spain*

[2] *ICMAB-CSIC, Campus UAB 08193-Bellaterra, Barcelona, Spain*

[3] *GES, UMR-CNRS 5650, cc074-Université Montpellier 2, 34095-Montpellier cedex 5, France*

[*] Corresponding author: nicolas.camara@imb-cnm.csic.es

Graphene has emerged recently as a new material with outstanding electronic properties. This includes mass-less Dirac fermions, ballistic transport properties at room temperature and good compatibility with the silicon planar technology. Graphene-based devices are then promising candidates to complement silicon in the future generations of high frequency microelectronic devices. Different techniques have been developed over the past 4 years to fabricate mono or bi-layers of graphene. They range from exfoliated graphite, either mechanically,[1] or in a liquid-phase solution,[2] to chemical vapor deposition on a metal surface,[3,4] and more recently, to substrate-free synthesis when passing ethanol into an argon plasma.[5] The method investigated in this work consists in a controlled sublimation of few atomic layers of Si from a mono crystalline SiC substrate.[6] Such epitaxial growth (EG) of graphene seems to be the most suitable option for industrial applications,[7] but for easy control, it necessitates large and homogeneous sheets of monolayer or few layers of graphene (FLG) covering either a full-wafer surface or a specific area of an AlN pre-patterned SiC substrate.[8]

Unfortunately, whatever the SiC polytype under investigation (4H, 6H or, even, 3C), or the sublimation conditions pressure varying from UHV (Ultra-High Vacuum) below 10^{-9} Torr to more standard SV (Secondary Vacuum) conditions in the range 10^{-8} to 10^{-6} Torr, it is still challenging to grow FLG with homogeneous domain sizes larger than few hundred nanometers.[9,10,11] However, sublimation from the C-face leads to wider domains and higher mobility than the Si-face, [10] but still, it is very challenging to process any set of homogeneous devices on the same wafer. A noticeable exception is the recent result by Emtsev et al.[12] that showed that performing graphitization on a 6H-SiC substrate under Argon at 900 mbar could lead to large, regular, graphene monolayers and bilayers, but unfortunately on the Si-face where the grown FLG mobility is lower. The purpose of this work is to show that there is an alternative way in which very large monolayer graphene ribbons can be grown on the C-face of a graphite-capped SiC sample using only a commercial radio frequency (RF) heated furnace under SV conditions, as normally used for SiC post-implantation annealing.

In such a way, increasing the temperature up to 1700°C, we found out that the intrinsic spontaneous growth is blocked while the nucleation procedure that originates from isolated surface defects is still activated, since less demanding in energy.[13] The increase of the Si partial pressure near the surface forced the graphene growth to expand more in 2 dimensions. It starts from the defect point and follows the natural SiC step structures that are ordered in long terraces. This results in the long graphene islands shown by Optical Microscopy in dark field mode Figure 1. They have the shape of ribbons, about 30 to 300 µm long depending on the processing time, surrounded by the SiC surface not yet converted in graphene.

Raman spectroscopy method was used to control the homogeneity of the ribbon. The spectra were collected at room temperature, in the confocal configuration using the 514 nm line of an Ar^+-ion laser as excitation wavelength. We obtained homogeneous Raman spectrum with a typical signature after subtraction of the bare SiC signal shown on Figure 2. The observed Raman signature of the ribbon is very close to the ones found in the literature for graphene monolayer exfoliated on top of SiO_2/Si. [14,15,16,17,18,19,20]

This work has been supported by EU in the framework of the MANSiC project Grant No. MRTN-CT-2006-035735.

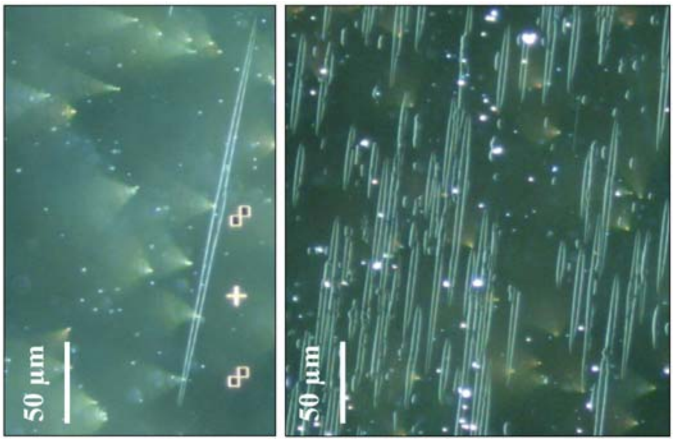

Fig. 1: Wide range Optical Microscopy view of samples covered by very long graphene ribbons from 30 to 300 µm long and 5 µm large depending on the sublimation time. Higher density of ribbons is encountered where higher density of defects on the surface of the SiC substrate.

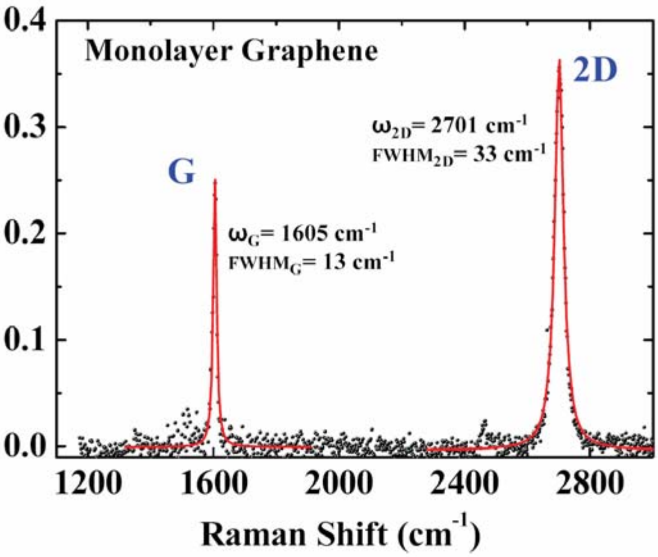

Fig. 2: Typical Raman spectrum of a monolayer graphene ribbon after subtraction of the SiC signal.

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Investigation of graphene growth on 4H-SiC

A. Castaing[1,*], O.J.Guy[1], M.Lodzinski[1], S.P.Wilks[1]
[1] *School of Engineering, Swansea University, Singleton Park, Swansea SA2 8PP, UK*
[*] Corresponding author :a.castaing.495707@swansea.ac.uk

Because of its outstanding electronic qualities, such as high structural integrity, zero band gap, massless carriers, large carrier mobility, long phase coherence length, and elastic scattering length, graphene has instigated research for a plethora of potential applications [1,2], such as nanoelectronics, nanosensors, photonics, single electron devices [3], spintronics, and interconnect applications. The physical properties of this one atom-thick crystal have made the study of graphene growth an important topic of both fundamental science and technological applications. Recently, low energy electron diffraction (LEED) [1] and scanning tunneling microscopy (STM) [4] have been used to analyse graphene sheets thermally grown on SiC (0001) surfaces by sublimating silicon from SiC substrates.

This paper reports X-ray Photoelectron Spectroscopy (XPS) analysis of the growth of graphene on 4H-SiC. The topography of the grown surfaces has been studied using AFM. Electrical characterization of the graphene layer's performance is also reported.

N-type 4H-SiC, Si-terminated, 8º off-axis samples, with a 10µm thick epitaxial layer and $1x10^{16}cm^{-3}$ doping density, purchased from CREE Research Inc., were used in this study. Samples were cleaned using a preliminary solvent and acid clean followed by a standard RCA clean. An HF dip was performed just before introduction of the samples in a UHV system ($2x10^{-10}$ mbar). Two different methods were used to grow the graphene layer: direct current heating and electron beam bombardment. The temperature was measured using an optical pyrometer. The XPS measurements were performed using a Vacuum Generator Escalab system equipped with a concentric hemispherical electron energy analyser and using the Al Kα-line of an X-ray source (1483.6 eV). Multiple scans of the C_{1s}, O_{1s} and Si_{2p} peaks were performed. A Veeco dimension Nanoscope IV was used for AFM measurements. The graphene/SiC samples were then covered with silver, deposited using a K J Lesker PVD75 sputtering system. The silver was then patterned lithographically to form equally spaced, aligned contacts (200nm thick, 100µm wide 1mm long, 1mm apart) to the graphene layer. Four point probe measurements were then performed on three different areas of the sample. I-V characteristics between each contact were performed.

The sample holder used to perform the direct current heating had a much larger ground connection than the live connection. This effectively acted as a heat sink at one end of the sample, allowing a graded variation in temperature along the length of the sample of about 100°C at temperatures above 1100°C. The increasing thickness of the graphene layer obtained along the sample has been determined using XPS data fitting (Fig. 1).

Electron-beam bombardment heating was performed using a low work function thoriated tungsten filament, whose electrons emitted were directed onto a molybdenum plate polarized at 1kV, on top of which the SiC sample was placed. This provided an uniform annealing of the sample. Fig.1 and Fig.2 clearly show the evolution and increase in intensity of the graphitic C_{1s} peak (peak G) with increased annealing, while the bulk SiC peak (peak S) becomes buried. The peak labelled X represents the interfacial carbon atoms in the graphene layer directly associated with the SiC substrate whereas, peak G is attributed to the graphene layers on top of this i.e. multi-epitaxial graphene (MEG) layers. The growth appears to be determined predominantly by the anneal temperature and is influenced less by the duration of annealing. Exposing the sample to air and then performing a subsequent XPS scan showed the sample surface to be almost unchanged, illustrating the chemical inertness and hydrophobic nature of the graphene layer. This also confirmed that there was at least one graphene layer all along the length of the sample, since SiC would have oxidized and an oxygen peak been

detected after exposure to air. AFM has been used to assess the topography of the graphene/SiC surface. The root mean square (RMS) roughness of the as-received 4H-SiC wafer was 0.72nm, whilst the RMS roughness of the graphene/SiC surfaces was 0.77nm. This indicates that the graphene follows the topography of the SiC substrate, and that the graphene growth process does not cause a significant increase in surface roughness.
Electric measurements were performed on different parts of both samples (Fig 2). These measurements give us for the direct current heating sample a sheet resistance between 770 Ω/sq and 10^4 Ω/sq and $4.5*10^3$ Ω/sq for the e-beam sample.

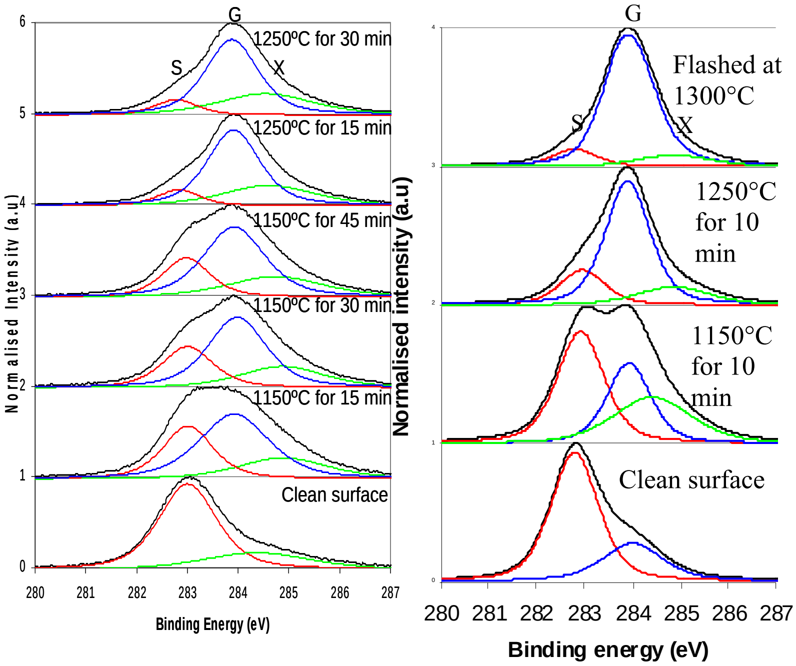

Fig. 1. Stacked, curve fitted plot of XPS data for the C1s peak, showing graphene growth during (a) direct current annealing from 1150°C to 1250°C, and (b) e-beam annealing from 1150°C to 1300°C

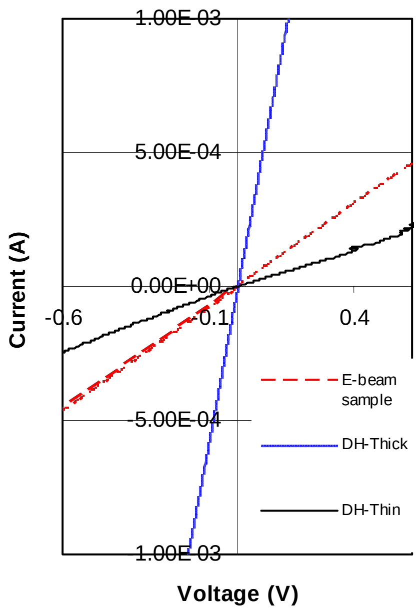

Fig. 2: Current versus voltage plot for the 4 points measurement, yielding the sheet resistance.

Thermal growth of graphene on 4H-SiC and XPS characterization of the evolving graphene layer has been performed. The introduction of a temperature gradient across the sample produces a set of graphene thicknesses ranging from one monolayer to tens of layers, as shown with electrical characterization. This method of graphene growth can be used for development of test structures whose properties are based on the thickness of the graphene layer, thus avoiding the fabrication of multiple graphene/SiC samples with different thicknesses. Once an adequate film thickness has been determined for the desired purpose, e-beam annealing can provide a more even sample for large scale purposes. No increase in RMS surface roughness of the surface was observed indicating that the graphene layer formed would not be disrupted by changes in the SiC substrate surface morphology (step-bunching) that occur at higher temperatures – used in graphene growth on SiC under lower level vacuum conditions.

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Nanoscale current transport at graphene/SiC interface by scanning probe microscopy

S. Sonde [1,2 *], F. Giannazzo[1], V. Raineri[1], R. Yakimova[3], J. Camassel[4]
[1]*CNR-IMM, Strada VIII , 5, 95121, Catania (Italy)*
[2]*Scuola Superiore di Catania, Via San Nullo, 5/i, 95123, Catania, Italy*
[3]*Department of Physics, Chemistry and Biology (IFM), Linköping University SE-581 83 Linköping, Sweden*
[4]*Université Montpellier 2, Place Eugène Bataillon 34095 Montpellier Cedex 5, France*
[*] Corresponding author: sushant.sonde@imm.cnr.it

Epitaxial graphene [1] (grown by solid state graphitization of SiC) has been shown, with recent advances in processing techniques, to have the potential in getting wafer size graphene needed for industrial application [2, 3]. Having said that, the crystal quality of mechanically exfoliated graphene is still better than epitaxial graphene. As has been shown, the epitaxial graphene always has the presence of buffer/transition layer in between SiC substrate and the first graphene layer. Depending on the substrate (Carbon terminated face of SiC (000-1) or Silicon terminated face of SiC (0001)) the successive grown layers show disorientation with respect to the reconstructed 6√3x6√3 under layer or are under compressive stress. Such effects result in the modification of electrical properties such as reduced mobility and changes in the electronic band structure of the grown layers of graphene [1]. Apart from that, graphene grown on SiC is superficially non-uniform, growing in sizes of ~2µm.
In the present work, we deposited graphene on SiC substrates with mechanical exfoliation. (Fig.1). Such deposited graphene presents a unique opportunity to compare the interface as well as electronic transport properties with the epitaxially grown graphene on SiC. The deposited graphene adheres well on to the SiC substrates and can be identified with optical microscope. The deposited flakes were characterized for thickness with tapping mode Atomic Force Microscopy (AFM). The morphological maps suggest that graphene follows the surface morphology of the underlying SiC substrate.
To investigate the graphene/SiC interface we made use of Conductive AFM (C-AFM) and Torsion TUNA (T-TUNA). Local C-AFM reveals that graphene forms an Schottky contact on SiC substrate. The current measured on an array of 25 tip positions on SiC is shown in Fig. 2 (a). Similar measurements carried out on graphene/SiC are shown in Fig 2 (b). As can be seen, presence of graphene lowers the barrier height of the Schottky contact on SiC. Also, it should be mentioned that the measured current characteristics are independent of the flake size. This is in accordance with the previously found observation that, a C-AFM tip forms an effective area (A_{eff}) on graphene flakes, which has a dependence only on the applied voltage. Being a Schottky barrier it is unlikely to see the variations in A_{eff}. The barrier height of the Pt tip/FLG/SiC system range between 0.5 and 1 eV, depending on the tip position on FLG.
The restriction posed by graphene on imaging force in both vertical as well as lateral direction doesn't allow using contact mode scanning of the flakes. To overcome this, we used Torsion-TUNA (Fig. 3) to collect current maps of the graphene deposited on SiC. With this technique it is possible to scan graphene for current maps by a non-destructive method. (Fig.4)

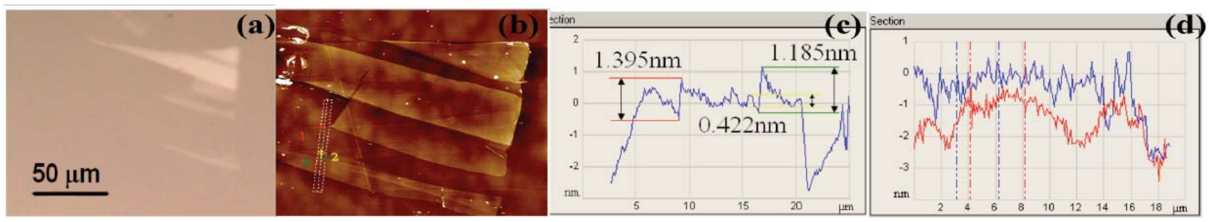

Fig.1: Graphene deposited on SiC showing optical micrograph in (a), tapping mode AFM micrograph in (b), an AFM linescan showing the relative thickness of deposited flakes in (c) and a linescan in (d) shows that graphene follows the surface morphology of SiC, the blue linescan is taken on graphene on SiC while the red linescan in taken on bare SiC substrate.

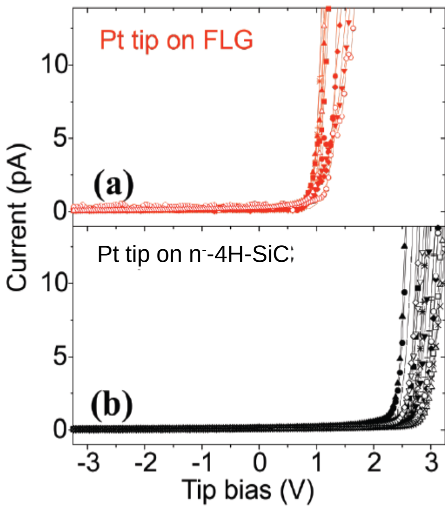

Fig. 2: An array of C-AFM carried out with a Pt coated Si tip measured (a) on few layer graphene (FLG) deposited on n^+4H-SiC and (b) on n^+4H-SiC.

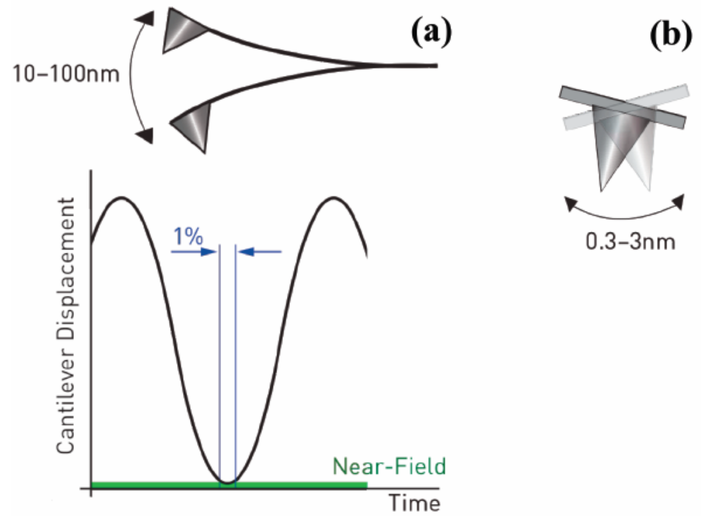

Fig. 3: A schematic comparing tip movements in (a) Tapping mode and (b) in Torsional resoance mode. The tip is in close proximity to the sample for approximately 1% of the oscillation cycle when using standard Tapping mode. In comparison the tip can be in close proximity to the surface all of the time when using Torsional resonance mode with small oscillation amplitude.

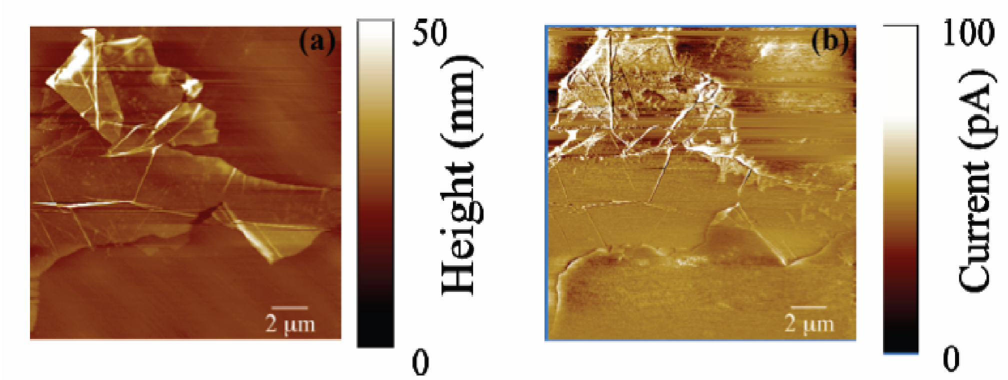

Fig. 4: Non destructive current mapping of graphene on SiC. Torsion AFM morphology is shown in (a), and the acquired corresponding current map on graphene in (b). The measured current amplitude depends on the underlying SiC surface morphology and the presence of graphene layers.

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Micro-Raman investigation of few graphene layers grown on 6H-SiC

Jean Camassel [1 *], Jean-Roch Huntzinger, Antoine Tiberj[1], Mikael Syväjärvi[2], Rositza Yakimova[2], Filippo Giannazzo[3]
[1]*GES, CNRS and Université Montpellier 2, 34095 Montpellier cedex 5, France*
[2]*IFM, Linkoping University, Linkoping, Sweden*
[3]*CNR –IMM, Strada VIII, 5, 95121, Catania, Italy*
[*] Corresponding author: jean.camassel@ges.univ-montp2.fr

Since the early work by Ferrari and co-workers [1] on few layers graphene (FLG) exfoliated on SiO_2/Si, Raman spectroscopy has become a most popular characterization tool to investigate FLG samples from different origins. In this work we focus on epitaxial graphene layers (ELG) grown on the Si face of a <0001>, 8°-off, 6H-SiC substrate. The growth was carried out in an inductively-heated reactor, operating at minimal pressure of $5x10^{-6}$ mbar. The growth temperature was 2000°C and, to lower the Si out-diffusion process, a confining argon pressure of 1 atmosphere was used [2].

EGL growth on the Si-face of <0001> SiC is a tricky process in which a preliminary surface reconstruction of the starting wafer is mandatory. Unfortunately, the reconstruction is hardly uniform. Given an off-axis angle, it proceeds through a complex admixture of step bunching and terrace enlargement such that, at the very end, only some terraces have reached the critical width for surface reconstruction [3]. This is probably the most intrinsic source of non homogeneity for EGL growth on SiC, but many others exist. They range from non perfect surface preparation before loading to non homogeneous thermal profile of the reactor. In this work, we have performed Raman investigations focusing on different areas of the sample shown in Fig.1.

We used a 514.5 nm laser line for excitation, and a T64000 confocal Raman spectrometer from Jobin-Yvon, with a x100 microscope objective leading to a ~ 1 µm spot size. We evidenced two different types of growth non homogeneities.

i°) At the cm scale, they are such that less graphene is usually found at the periphery of sample (data points “b” and “c”) than displayed at point “d” or in the center zone “a”. Despite the use of highly isothermal conditions to insure homogeneity, this may come from a not yet perfectly optimal design of the reaction chamber or from a lack of suitable surface preparation like Epiready® polishing by Novasic before loading in the reactor. In both case, this should not be so difficult to cure. At the present time and for electronic device applications, this simply means that defining some exclusion zone at the periphery of sample is a pre-requisite.

ii°) At the microscopic scale, the problem is more serious. This is shown in Fig.2 and might not be so easily solved.

We focus now in the central window “a”, from data point “aa” to “ae”. The change in brightness in Fig.1 is indicative of a change in local graphene coverage, from very thin for the dark stripes to thicker for the lighter ones. In Fig.2, this manifest as a more or less intense G band, superimposed on the 2-phonons signal of the 6H-SiC substrate, together with a 2D band which is too broad to correspond with monolayer (ML) graphene [1]. In fact, within few micrometers we find then that the *average* graphene thickness probed by the Raman spot can change very rapidly from less than 2 MLs (for spot size position “aa”) to thicker FLGs (for spot size position “ae”) and even thicker values (for spot size position “ac” and “ad”).

Such microscopic homogeneities do not come from a design problem. They come from the intrinsic surface reconstruction aspects. At the present time it is not clear whether an improved surface polish before loading in the reactor could improve the final results, or not. This will have to be investigated before large scale electronic applications can be done.

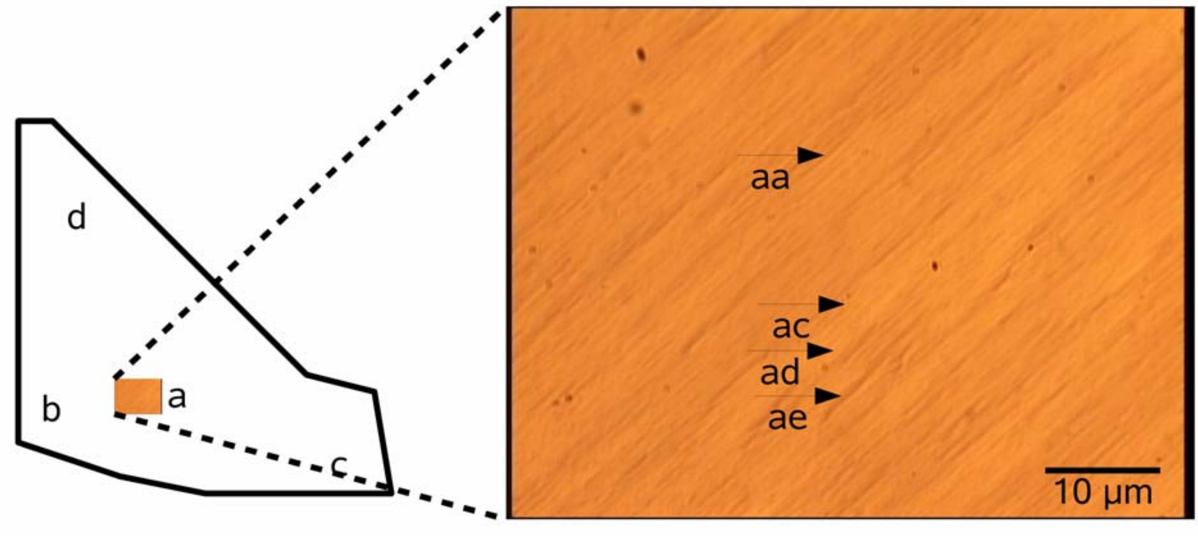

Fig.1 Schematics of the FLG sample investigated in this work, with expanded microscope view.

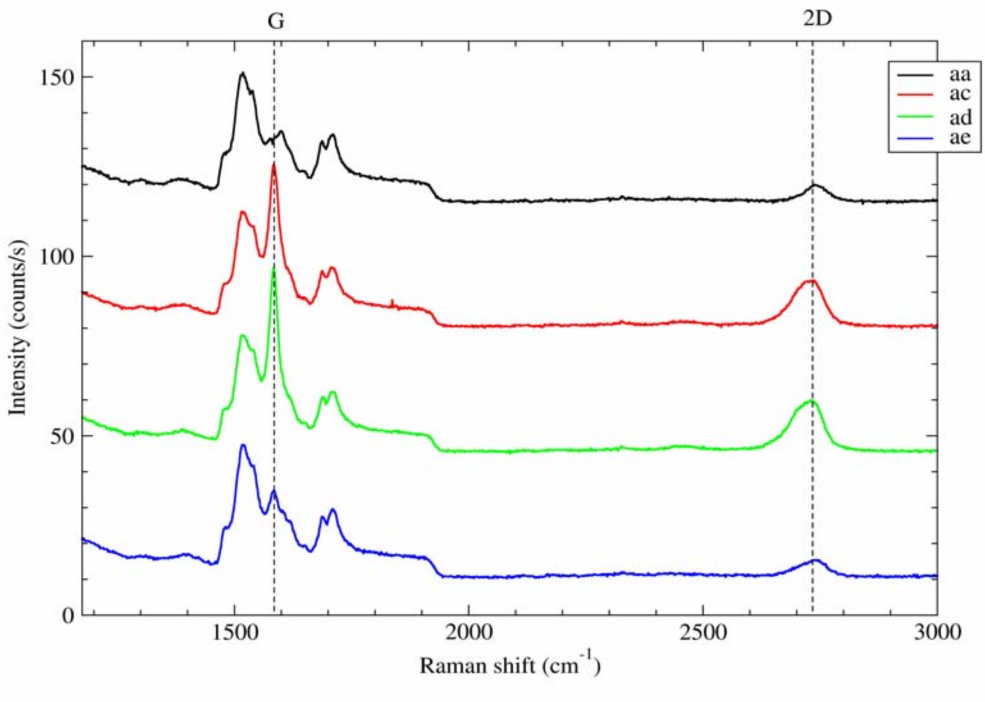

Fig.2. Raman spectra collected at different points labeled “aa” to “ae” in Fig1 (see text).

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Silicon Carbide 3C/6H heterointerfaces

M. Spencer *, MVS Chandrashekhar, Jie Lu, Chris I. Thomas,
Department of Electrical and Computer Engineering Cornell University, Ithaca, New York, USA
* Corresponding author: spencer@ece.cornell.edu

Arguably the most unique property of Silicon carbide (SiC) is it's ability to form in different polymorphs which have distinct electronic properties. In this work we investigate SiC 3C/6H heterointerfaces. Cubic Silicon carbide hetero-polytype junctions have been fabricated on the C face of 6H-SiC. These junctions although unintentionally doped, form two dimensional electron gas (2-DEG) structures because of the strong spontaneous polarization present in the hexagonal polytypes of SiC. In this work we present the fabrication, and characterization of SiC heteropolytpe junctions. As part of this work measured values of the spontaneous polarization of 6H-SiC are compared to theoretical predictions.

Silicon carbide (SiC) has been studied intensively due to the potential for high voltage, high power and high frequency devices [1]. The material has over 250 polytypes of which the common polytypes are 3C(cubic), 4H(hexagonal) and 6H(hexagonal). The hexagonal polytypes exhibit spontaneous polarization unlike the cubic polytype [2]. Cubic (3C-SiC) grown in the <111> direction is lattice matched in the <0001> plane of 6H-SiC to within <0.1%. In addition 3C and the hexagonal polytypes (4H and 6H) are thermally matched to <0.1% over the entire range of measurement and sample preparation temperatures [3]. This matching enables a new class of chemically homogeneous heterostructures formed only by an abrupt change in crystal structure and/or stacking, rather than an abrupt change in composition, such as in the GaAs/AlGaAs material system. Cubic (3C-SiC Bandgap, Eg=2.36eV) and 6H-SiC (Eg=3.0eV) have a large conduction band offset (0.7eV). The change in the spontaneous polarization at the cubic hexagonal interface leaves a fixed positive charge on the C-face of <0001> 6H-SiC, electrostatically inducing a mirror electron charge, which is then confined by the band offset effectively "doping" the junction and producing a 2-DEG [4-6]. If the growth of cubic material is performed on the silicon face of 4H or 6H a hole gas is predicted to result. The SiC epi-layers reported in this study were grown on the C-face of either n^+ or semi-insulating 6H-SiC singular substrates with a mis-orientation of at most .2 degrees (in random orientation as measured by the vendor). The growth was performed in a vertical cold-wall chemical vapor deposition (CVD) reactor. Silane, propane and HCl were the reactant gases while hydrogen was used as the carrier gas. An unintentionally doped 6H-SiC buffer layer ($\sim 2 \times 10^{17} cm^{-3}$ n-type as determined by capacitance voltage measurements) and 3C-SiC hetero-layers were formed at a temperature of approximately 1350^0C and a pressure of 600 Torr. The growth rate was approximately ~0.8um/hr. It was observed that the growth of hexagonal SiC occurred at temperatures in excess of 1350C° for the growth conditions investigated. The surface morphology of the cubic SiC indicated island growth. High quality heteropolytype interfaces could be prepared by using a temperature ramp down technique similar to that discussed by Neudeck et. al [7]. This technique produced island sizes as large as 30 microns. It was determined that films grown using the temperature ramp down technique contained a 6H-SiC buffer layer followed by a thin 3C-SiC layer. The 6H-SiC buffer layer was produced in the initial stages of the temperature ramp at temperatures in excess of 1350C° while the 3C-SiC layer was produced at later stages in the temperature ramp when the temperature was low enough to suppress step flow growth. Capacitance-voltage (C-V) techniques were used to investigate the doping and polarization properties of the heterojunctions. Ti/Au (20A/1500A) dots for the Schottky contact were evaporated on the top of 3C-SiC by electron-beam evaporation using a shadow mask. The diameters of the Schottky contacts were 150-300um. C-V measurements were performed at low temperatures 4K-100K.

A two dimensional electron gas (2DEG) was observed in C-face 3C/6H SiC polytype heterostructures by C-V (capacitance-voltage method). The carrier density of the 2DEG in the best samples was found to be $2.5x10^{12}/cm^2$. By semi-classical analysis of the electrostatics, we extracted the spontaneous polarization charge and determined that in 6H-SiC the polarization charge was $3x10^{12}/cm^2$. This value quantitatively agrees (within 20%) with previous measurements of the polarization charge in 4H-SiC [8], (as inferred from optical measurements of 3C/4H stacking faults) and is found to be lower than the theoretically predicted values of spontaneous polarization by about 300%. Hall samples were fabricated in order to investigate the 2-DEG mobility. Phosphorus implanted contacts were activated at $1350C^{\circ}$. The wafers were then fabricated in the Hall bar geometry with high-purity Ni Ohmic contacts alloyed at $1000C^{\circ}$. Hall bar geometries with lengths of 100μm and widths of ~5μm were used. Conventional low field hall was performed as a function of temperature at low magnetic field. These results showed the presence of 2-DEG. In order to confirm the low field measurements magnetotransport measurements were performed over the magnetic-field range of 0–10 T and temperatures 1.5 K to 100 K. Fig. 1 shows the as-measured magnetoresistance as a function of magnetic field at 1.5 K, plotted as the derivative of R_{xy} and R_{xx} (which is taken with respect to magnetic field) in order to clearly identify the periods the quantum Hall plateaus in R_{xy} and Shubnikov-de Haas (SdH) oscillations in R_{xx} as a function of 1/B . The QHP and SdH oscillations show the presence of a well-confined 2DEG. The measured mobility of the 2DEG is $2000cm^2/Vs$ (at 4K) with an electron sheet density of $2.7x10^{12}/cm^2$. The independent measurement of sheet density agrees well with the C-V result.

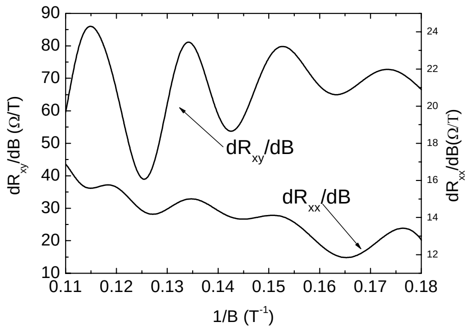

Fig. 1: Longitudinal magnetoresistance R_{xx} (d(R_{xx})/d(B) and transverse magnetoresistance R_{xy} (d(R_{xy})/d(B)) in 3C/6H SiC heterostructures as a function of magnetic fields normal to the heterointerface at 1.5 K. as a function of 1/B, after FFT smoothing.

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Multiscale graphene quantum transport modeling and issues: the case of graphene epitaxially grown on SiC (0001)

I. Deretzis[1,2*], A. La Magna[2]
[1]*Scuola Superiore, Università di Catania, 95123 Catania, Italy*
[2]*CNR-IMM, 95121 Catania, Italy*
[*] Corresponding author: ioannis.deretzis@imm.cnr.it

The purpose of this study is to implement a bottom-up multiscale approach on the modeling of graphene-based systems, from density functional to semiempirical with different levels of accuracy (Extended Hückel with various bases and parameterizations and Tight-Binding). We start-off considering graphene-based quantum dots[1] with a hexagonal symmetry as a case-study. Using the ab initio calculations as a reference, the goal is to recognize the theoretical framework under which semiempirical methods describe adequately the electronic structure of the studied systems and thereon proceed to the calculation of quantum transport within the non-equilibrium Green's function formalism. Our analysis shows that deviations from the ideal two-dimensional honeycomb lattice (confinement, substrate induced scattering potential, vacancies and hydrogen impurities) challenge the traditional tight-binding picture of graphene-based complexes whereas the role of parameterization proves to be crucial even within the same semiempirical context. In terms of conduction, failure to capture the proper chemical aspects in the presence of generic local alterations of the ideal atomic structure sketches improperly the transport features, while contrary, a correct treatment of the latter by the semiempirical models can lead to massive transport calculations of realistic graphene-based devices. As an example, we show wavefunction localizations provoked by the presence of vacancies (figures 1-3), and how important is their modeling for the conduction characteristics of the studied systems.

We thereon follow the same methodological procedure in order to investigate quantum transport features of armchair graphene nanoribbons epitaxially grown on SiC (0001) surfaces. An atomistic description of both device and substrate to the best possible extend takes places here. The evaluation of the semiepirical methods is based on first principles bandstructure calculations, and as soon as the most adequate semiempirical method is identified, we proceed with the calculation of transport. Using a fully quantistic description of the device coupled to a three-dimensional Poisson solver we account for effects like charging and screening under non-equilibrium conditions[2-4]. Results demonstrate, considering the particular reconstruction case, a tight chemical bonding, and a consequent alteration of the electronic structure and transport, between the first graphene layer and the Si atoms of the SiC substrate, whereas typical graphene-type conduction features are recovered with the addition of a second graphene layer.

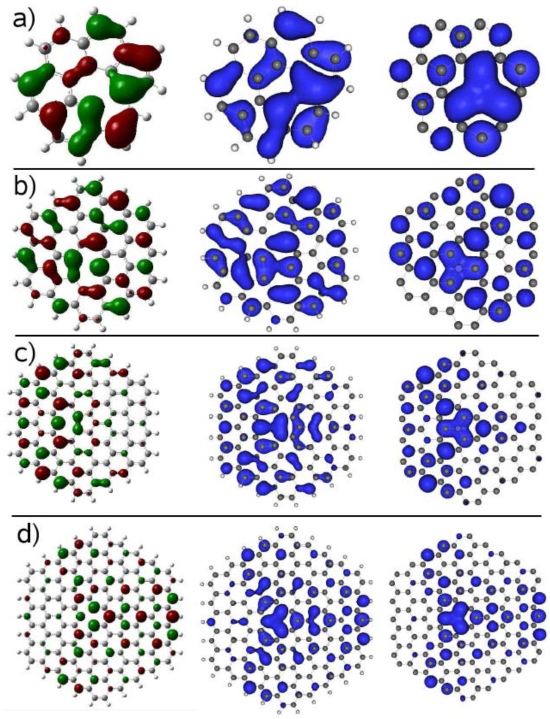

Fig. 1: HOMO molecular orbitals for a) n=2, b) n=3, c) n=4 and d) n=5 coronene molecules with a single vacancy by means of DFT-GGA (left), Extended Hückel (middle) and Tight-Binding (right).

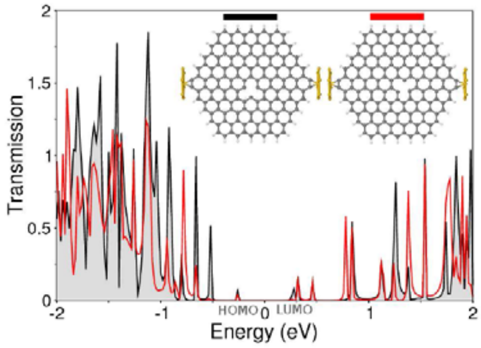

Fig. 2: Transmission as a function of energy by means of the Extended Hückel method for two equivalent contact configurations that differ only in the position with respect to the defected site.

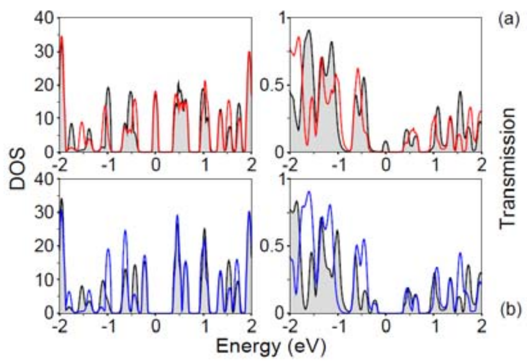

Fig. 3: Density of states and transmission probability by means of the Tight-Binding method for nonparameterized (a) and parameterized (b) vacancy values.

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Technology and Product trend of SiC Power Semiconductors at Infineon

R. Rupp[1*], F. Björk[2], M. Treu[2]
[1]*Infineon Technologies AG, Am Campeon 1-12, 85579 Neubiberg, Germany*
[2] *Infineon Technologies AG, Siemensstrasse 2, 9500 Villach, Austria*
[*] Corresponding author: roland.rupp@infineon.com

Power supply manufacturers in computing, communications and industrial area are under continuous pressure to increase system efficiencies, driven by the demand for lower operating costs, energy initiatives such as Energy Star [1], or via legislations. Since system cost per watt is typically not allowed to rise, increasing efficiency puts tough demands on semiconductor and passive component performance as well as topology innovation.

Silicon Carbide (SiC) as ideal semiconductor material for low loss power electronics is playing an important role with respect to this trend since the initial commercialisation of SiC power devices in 2001 [2]. Those 1st devices have been high voltage Schottky diodes (300V – 1200V), and still such diodes are the only commercial SiC devices in early 2009. This does not look like a technology with a high innovation rate, as it would be expected, when moving to a completely new power semiconductor material. But when looking into more detail and comparing those 1st diode products from 2001 with the recent (meanwhile 3rd Generation) products, it becomes obvious, that some significant innovation happened in between:

- Production in 2001 started on the basis of 2” SiC wafers, with an in-between step on 3” in 2004, since beginning of 2009 the manufacturing transfer to 100 mm SiC wafers is completed.
- Today’s costs for a 100 mm SiC epi wafer are pretty close to the 2” epi wafer costs in 2001 which had less than a quarter of the area. This means, that with respect to affordability of the SiC technology some tremendous achievements have been made.
- On device level a 3rd Gen SiC Schottky diode of Infineon has only little similarities to it’s “ancient” counterparts from 2001:
    - First Generation Schottky diodes have been plain Schottky diodes already providing low switching losses by the absence of minority carrier injection but suffering from much lower surge current capability than the Si based competition parts and showing high sensitivity against overvoltage surge and high dV/dt transients.
    - Second Generation Diodes contain a merged pn-Schottky (MPS) structure, not for the purpose of leakage current reduction but for playing an active role for improving surge current stability by minority carrier injection in this surge mode. By a smart design of the MPS cell design, it was possible to achieve this without increasing the active area of the devices or increasing V_f at nominal current, despite the area consumption by the p-areas. As an additional benefit of the MPS structure those devices are now also very rugged against overvoltage spikes by showing nice and stable avalanche operation with a positive T-coefficient [2]. Also the edge termination structure was improved in a way, that even extreme dV/dt in the range of 100V/ns and more can easily be handled. Meanwhile a test to insure this also for continuous operation is part of our standard qualification procedure.
    - The recently launched 3rd Gen SiC diodes still consist of a MPS structure. The major innovation this time comes from the die attach inside the package. At Infineon we have succeeded to develop a “solder-free” die attach process to the copper leadframe which eliminates the main barrier for the heat flux from the active area of the device to the heat sink [3]. By this measure, $R_{th,jc}$ was reduced by more than 40% for a given chip size allowing a further increase in

power density (i.e. current density) in the diode chip. This not only supports further cost reduction but also helps to decrease the diode capacitance and therefore the capacitive switching losses significantly (see fig 1). At switching frequencies of 130kHz this leads to another 15-20% reduction of the total diode power losses under low to medium output power conditions in power supply applications (typical operation), another nice customer benefit!

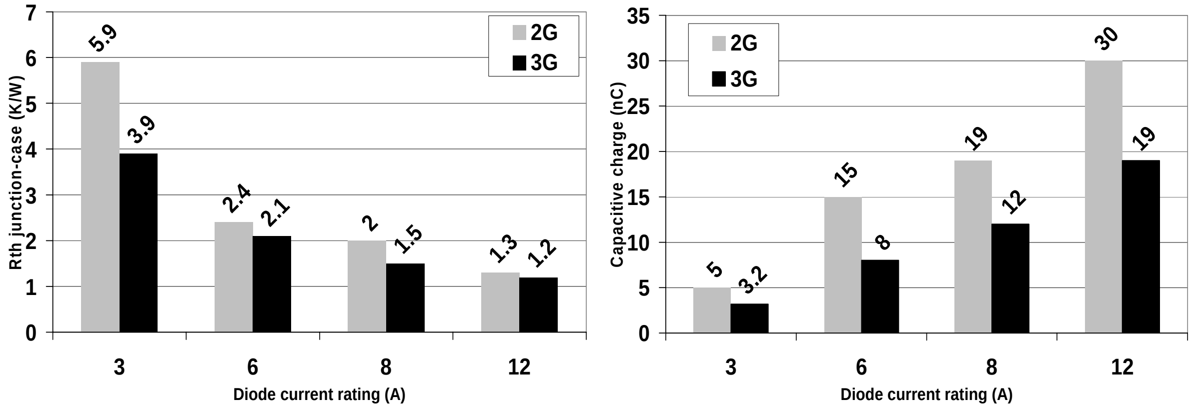

Fig. 1: Improvement of thermal resistance chip junction-to-case ($R_{th,jc}$, left) and device capacitances (right) for second and third generation SiC diodes. (Please note, that diodes with same current rating are compared, not with same active area!)

As of today there are still plenty of options to further improve the SiC diode benefits and cost position, therefore it can be expected that the penetration of SiC in the high performance diode market will continue with rapid pace. But what about the market entry of a high voltage SiC power switch?

Still the race between the various switch concepts like MOSFET, BJT and JFET is not decided and even outside SiC GaN-HEMT based power switches have been considered as potentially strong competitive technology.

Within Infineon we favour a JFET (Junction Field Effect) power switch concept in SiC, which does not require a gate oxide and offers superior ruggedness in many application aspects (e.g. ESD, avalanche, short circuit conditions). However, this device is normally on (conducting without gate voltage), when best cost/performance is the target. This feature can be addressed with the help of a cascode configuration employing a low voltage MOSFET to generate the necessary voltage drop along the MOFET source-drain path to pinch the JFET off [4]. For the SiC JFET very attractive area specific on resistances have already been achieved: < 6 mOhm*cm² for devices with 1200V blocking. But also the SiC MOSFET is still on our R&D roadmap together with our SiC development partner SiCED.

It is not yet decided when Infineon will launch a SiC power switch product portfolio, the main activities today are focused in translating the existing technology into a easy to use and affordable customer solution.

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Reduction of leakage current in MOSFETs fabricated on 3C-SiC substrate

H. Nagasawa[1,*], T. Kawahara[1], N. Hatta[1], K. Yagi[1], M. Abe[1], B. Zippelius[2], G. Pensl[2]
[1]*SiC Development Center, Hoya Corporation, 1-17-16 Tanashioda, Sagamihara, Kanagawa 229-1125, Japan*
[2]*Lehrstuhl für Angewandte Physik, Universität Erlangen-Nürnberg, Staudstr. 7/A3, 91058 Erlangen, Germany*
[*] Corresponding author:

3C-SiC is a promising material for power MOSFETs with switching capability around 600 V to 1200 V, due to its lower interface state density at MOS interfaces [1,2]. n-channel vertical MOSFETs with specific on-resistance of 8 mΩ-cm^2 were realized on 3C-SiC substrates [3]. They demonstrate normally-off switching operation up to 200°C. The effective operating area with 2 mm^2 conducts 10A of drain current at a drain-voltage of 4V and a gate-voltage of 15V. This smaller operating area reduces the capacitance in MOSFETs resulting in higher switching speed. The channel mobility attains 220 cm^2/Vs at a gate voltage of 10V. This brings about remarkable reduction of specific on-resistance. Above results clearly prove the advantage of 3C-SiC as a substrate for power MOSFETs.
The serious problem at present is the leakage current through source-drain at reverse bias [4]. In order to focus on the leakage current at pn junction, vertical pn diodes with various sizes shown in Fig.1 were characterized. As shown in Fig.2, the leakage current density shows a non-linear dependence on the reverse bias voltage. The dependence of leakage current on bias voltage changes with operating temperature suggesting that a certain activation process of electrons generates predominantly the leakage current.
In order to make sure the origin of leakage, a pn diode with higher leakage current was investigated by combining electron beam induced current (EBIC), and photo emission microscopy (PEM) [5]. As shown in Fig.3, SFs can be observed as horizontal or vertical lines by EBIC image. Simultaneously, a specific SF which generates leakage current can be ascertained by superimposed PEM image. This SF exposes C-face on (001) surface crossing the pn junction.
The leakage current at the pn junction strongly depends on the SF density as shown in Fig.4. For example, an one order of magnitude increase in the SF density enhances the leakage current five orders of magnitude. This dependence suggests an upper limit for the SF density of 1x10^4/cm^2 for realizing MOSFETs with practical use.
At the workshop, the mechanism of the leakage current will be discussed with respect to the dependence on SF density, reverse bias voltage, and operating temperature. Finally the latest result of leakage current reduction in 3C-SiC junctions with lower SF density will be reported.

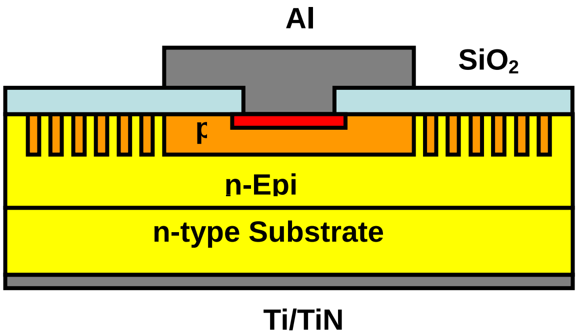

Fig. 1: Cross-sectional structure of a pn diode: An Al implanted 1um-depth box profile with $1x10^{18}/cm^3$ is fabricated in n-type epitaxial layer with $[N]=7x10^{15}/cm^3$. The diode is surrounded by six guard rings with 1um-width. Al electrode is contacted to 0.2um-thick p^+ layer with [Al] = $1x10^{20}/cm^3$.

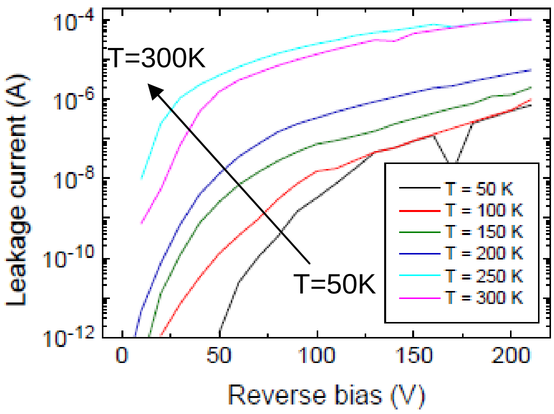

Fig. 2: Changes in leakage current as a function of the reverse bias voltage at various operating temperatures.

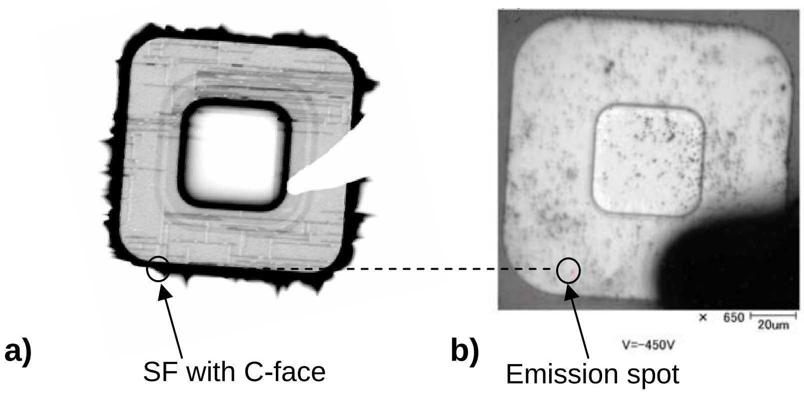

Fig. 3 a) EBIC and b) PEM image. A PEM spot located just on a SF which exposes C-face crossing the pn junction.

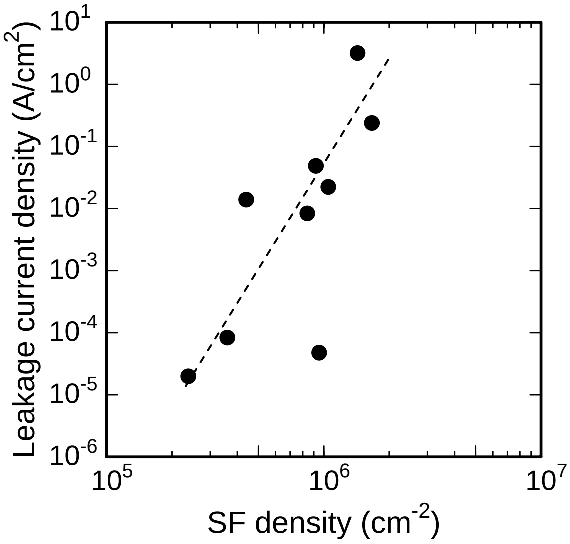

Fig. 4: Change in leakage current of a pn diode as a function of SF density. An one order of magnitude increase in the SF density enhances the leakage current five orders of magnitude.

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Optical investigations techniques used for stacking faults characterization in SiC

S. Juillaguet *, T. Robert, J. Camassel
Groupe d'Etude des Semiconducteurs, Université Montpellier 2 and CNRS,
cc 074-GES, 34095 Montpellier cedex 5, France
* Corresponding author: juillaguet@ges.univ-montp2.fr

Stacking Faults (SFs) are important crystal defects in 4H-SiC [1]. They can be electrically active and, in this case, behave as deep quantum well (QW) traps for electrons [2]. This leads to the degradation of high voltage bipolar diodes [3].

The basic origin of SFs in SiC is the small total energy difference between two different polytypes. The net consequence is that they can appear spontaneously, during the growth or after any mechanical or electrically stress. In 4H or 6H-SiC they manifest as a stable lamella of a different polytype, in most cases 3C-SiC [1, 4-5]. 8H-SiC has also been identified [6] but, mainly, for in-grown SFs in 4H-SiC.

Whatever is the faulted polytype, a SF is always associated with a finite thickness and a finite lateral extension in the basal plane. Since the faulted polytype has a smaller bandgap than the one of the host material, they behave like thin natural type-II quantum wells (QWs) embedded in the 4H-SiC matrix.

The binding mechanism comes from the difference in intrinsic band offsets and (internal) lattice polarization between the well and barriers [1, 6]. The difference in internal polarization not only participates in the binding mechanism, it also induces an internal macroscopic electric field in the wells [7, 8].

The experimental value has not yet been exactly determined [9] but the corresponding quantum confined Stark effect lowers the energy of the electrons in the well, the holes remaining in the outer barriers. The QWs are therefore of type II and, at low temperature, the Coulomb interaction binds together to different series of electron-hole (e-h) pairs [10].

The concept of "optical SF signature" comes from the LTPL (Low Temperature PhotoLuminescence) measurements [11] in which regular series of broad, regularly spaced, series of lines have been identified. A typical example is shown in Fig.1. It is extracted from a previous work [9, 12] and concerns 8H SF-QWs in a 4H-SiC matrix.

At 5K, the LTPL spectrum displays four large lines, noted LO, TO, LA and TA. They are indicative of phonon-assisted radiative recombination processes and the corresponding excitonic energy gap (E_{gX}) is equal to 2.672 eV. From TEM results [11] we know that this optical SF signature is associated with a 8 bilayers (BLs) thick 8H lamella which comes from a double combination of double SFs of the type 4SSFs(4,4). For details, see Ref.[13]. Moving from 8H-SF to 3C-SF and even changing the well polytype, not much varies. The only sensitive parameter is the change in energy position of the SF signature which, for a given polytype, should be a direct function of the QW thickness.

In this work, we present a review of recent LTPL, cathode-luminescence and micro-photoluminescence studies that help finding the experimental values of such parameters. For different polytypes and different acquisition conditions, we discuss the optical signature and compare with the result of model calculations. Since a SF is always a finite ribbon of 3C or 8H polytype in a 4H or 6H matrix, with a slightly different crystalline structure but a different internal polarization field, we take successively into account the effect of valence band offset, internal polarization and non homogeneity of the potential well. Finally, in the case of cathodo-luminescence and micro-photoluminescence techniques, we show that some screening of the built-in electric field can be reached.

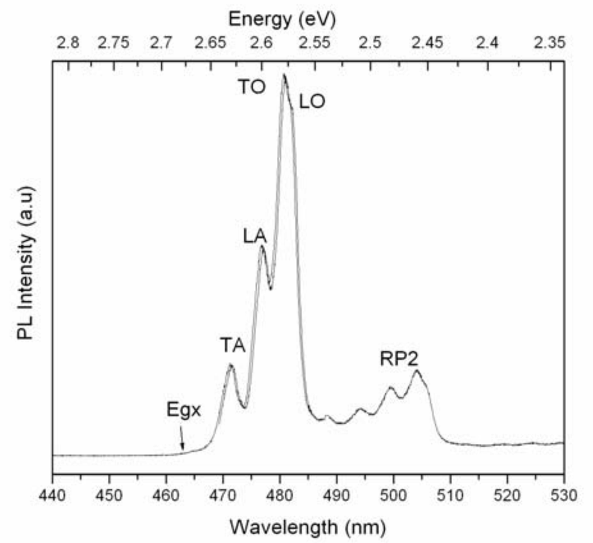

Fig. 1: LPTL spectrum collected at 5K on an in-grown stacking fault in a 4H-SiC epitaxial layer. One phonon (TA, LA, LO, TO) and two-phonon assisted recombination lines (RP2) manifest. The optical SF signature is ~ 2.672 eV.

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Development of Methods for Dislocation Characterization in SiC Materials and Devices

M. Dudley *, N. Zhang, Y. Chen
Department of Materials Science and Engineering, Stony Brook University, Stony Brook NY 11794-2275, USA
* Corresponding author: mdudley@notes.cc.sunysb.edu

The broader implementation of SiC based devices continues face significant barriers arising from defects. Developing nearly-perfect SiC epitaxial layers relies on understanding of the defect distributions in the Physical Vapor Transport (PVT) grown substrates and their behavior at the substrate/Chemical Vapor Deposition (CVD)-grown-epilayer interface. Synchrotron X-ray topography has played a strong role in achieving such understanding and in recognition of this a review is presented of recently developed white and monochromatic synchrotron radiation topography methods which enable dislocation characterization in SiC single crystal substrates, epilayers and devices. The methodologies used in applying these techniques to gain understanding of the origins of the defect distributions and how they evolve during PVT substrate growth and CVD epilayer growth will be discussed. This will include information on determination of dislocation Burgers vector (magnitude and sign), and line direction by comparison of observed images and those simulated using a ray tracing approach. Also, criteria applied to analyze the configurations of the various dislocations so as to provide insight as to whether they are “growth” dislocations or if they result from dislocation glide under stress will be outlined. Application of the various techniques to the complete analysis of substrate dislocations including c-axis threading screw dislocations (TSDs; both hollow and closed-core), basal plane dislocations (BPDs), and threading edge dislocations (TEDs) will be discussed. TSDs are shown to be growth dislocations and both the magnitude and sign of their Burgers vectors can be determined [1,2] (Fig. 1). Various nucleation mechanisms for TSDs will be discussed [3,4]. For TEDs we will show that there are six kinds [5] (Fig. 2). TED nucleation, both individually, and as groups aggregated into small angle boundaries, will be discussed. For BPDs, we will discuss their nature (Fig. 3) and generation mechanism during physical vapor transport growth of the substrates (Fig. 4). The mechanism by which BPDs can be converted into TEDs during epilayer growth will be discussed. We will also show how screw oriented BPDs tend not to convert into TEDs but replicate into epilayers. Such screw oriented BPDs in the epilayers can be forced to glide sideways under the influence of mismatch induced stress leading to the generation of misfit dislocations at the substrate epilayer interface. We will show how the continued glide of the screw oriented BPDs during growth can lead to the creation of half loop arrays [6]. In addition, we will show how TSDs can be converted into Frank partial dislocations and Frank faults during epilayer growth [7] (Figs. 5 and 6). This is shown to be a result of the interaction between vicinal steps and the spiral steps associated with the surface intersection of the TSDs which can lead to either accumulation or reduction of Burgers vector. We also demonstrate that scratches on the substrate surface can act as dislocation nucleation centers during CVD growth.

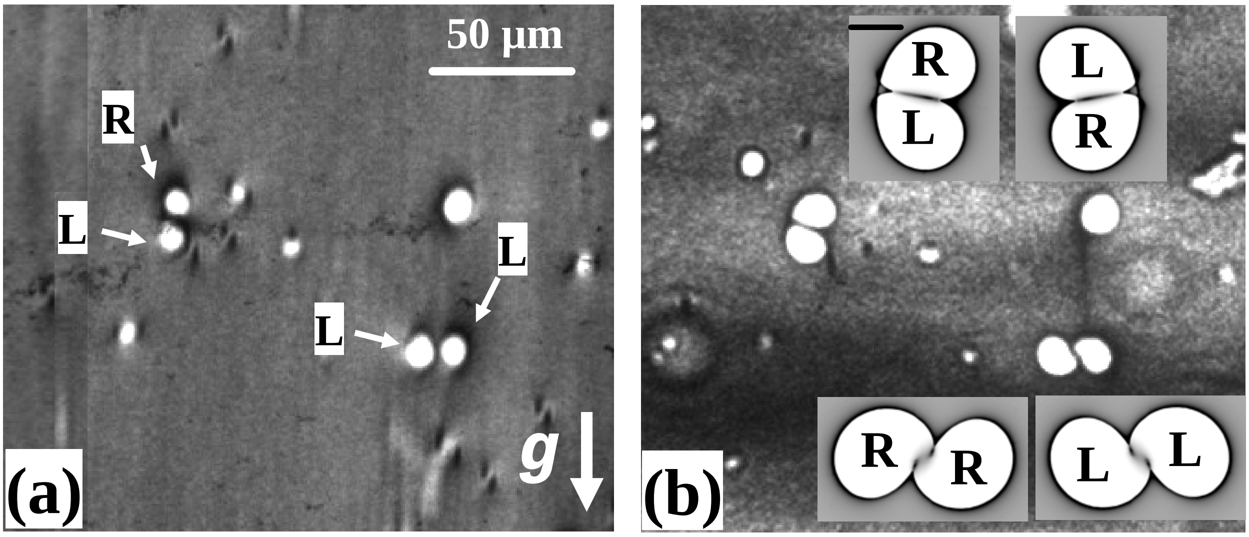


Fig. 1: X-ray topographs recorded using monochromatic synchrotron radiation from a 4H-SiC substrate. (a) recorded in grazing incidence; (b) recorded in back reflection (insets show simulations). Detailed ray tracing simulations enable determination of both the magnitude and sign of the TSDs. L indicates left-handed, R right-handed.

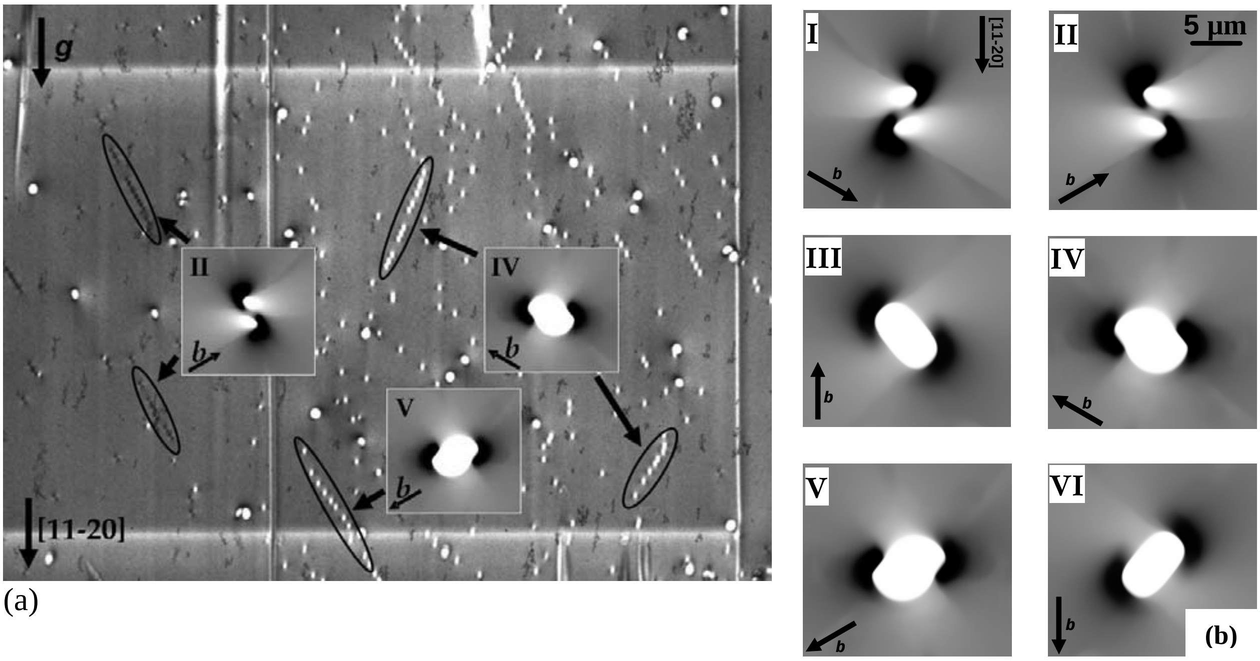


Fig. 2: (a) 11-2 12 Grazing incidence monochromatic image recorded from an epilayer grown on a 3 inch, 4H-SiC wafer showing TSDs and six different kinds of TEDs some of which aggregate into small angle boundaries; (b) simulations of the six types of TED.

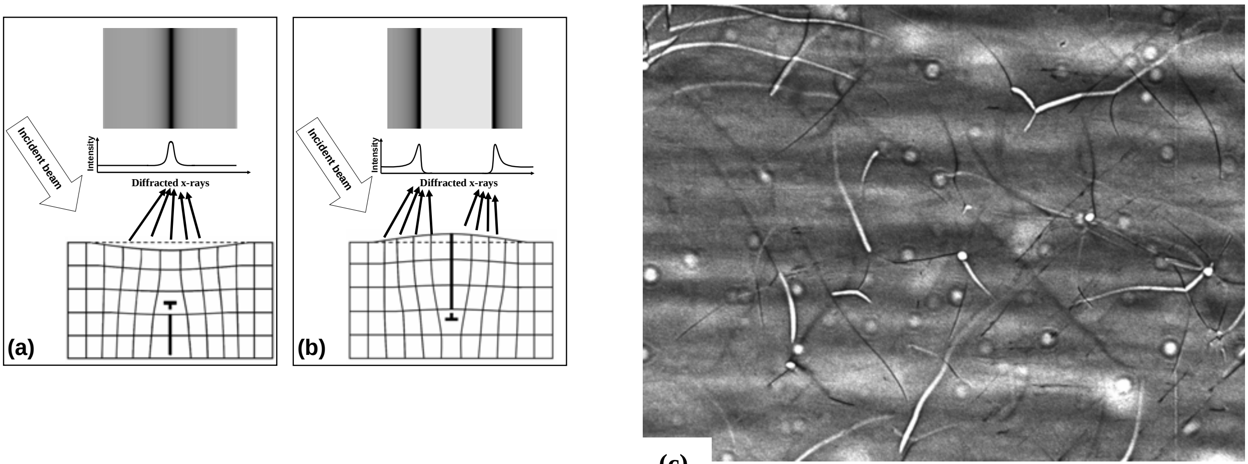


Fig. 3: (a) and (b) Schematics of back reflection ray tracing simulations of BPDs in 4H-SiC. Simulation enables determination of both the sign and magnitude of the Burgers vector of the BPDs plane dislocations which appear as narrow dark lines or broad white lines with dark borders on the back reflection image (c).

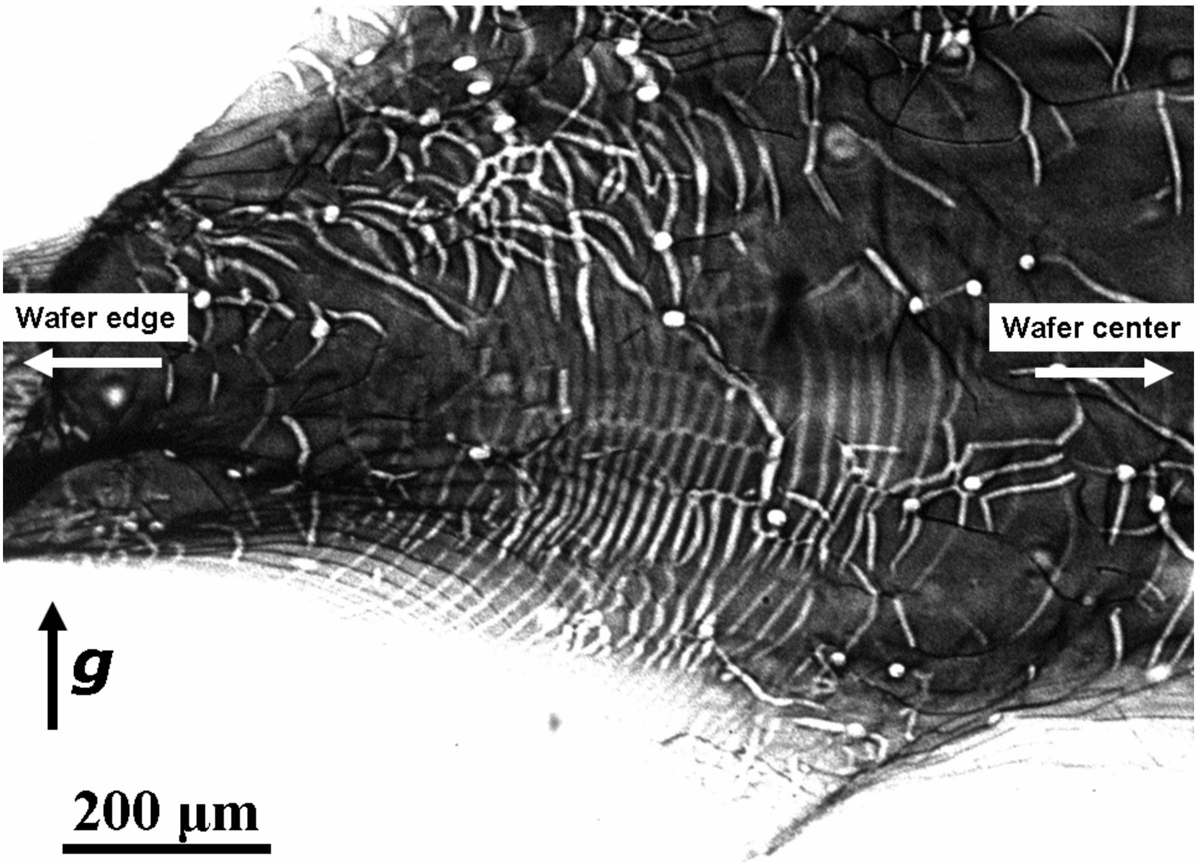
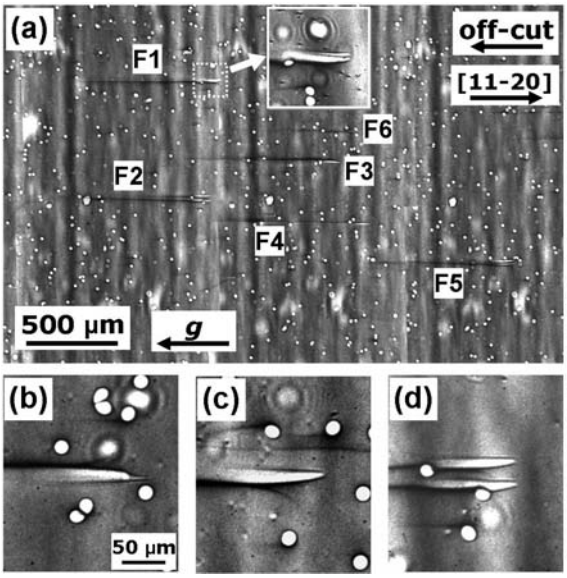


Fig. 4: Monochromatic topograph recorded from a 4H-SiC substrate. Note the concentric loops of white contrast BPDs which indicate that they are all of the same sign and that they are formed via deformation processes that occur near the wafer edge and propagate towards the wafer interior.



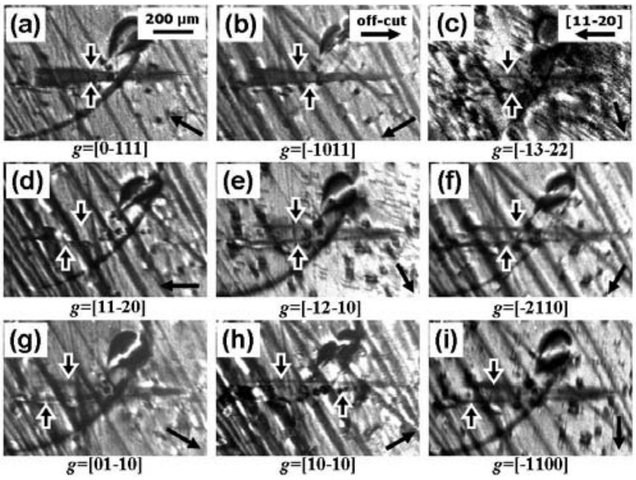


Fig. 5: Back reflection image recorded from a 4H-SiC epilayer showing TSDs and various combinations of Frank partials and Frank faults (F1-F6) created by deflection of TSDs onto the basal plane at the epilayer interface.

Fig. 6: Series of transmission topographs confirming the nature of the Frank partials and faults. The partial dislocations are out of contrast when **g . b**=0 and **g . b x l**=0, where g is the reflection vector, b is the Burgers vector and l is the line direction. The stacking fault is out of contrast when **g . R** = 0, where **R** is the fault vector.

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Optical characterization of wide bandgap semiconductors at excitation conditions approaching a power device operation

K. Jarašiūnas*, T. Malinauskas, R. Aleksiejūnas, S. Nargelas, P. Ščajev, G. Manolis, and V. Gudelis

Division of Optical Diagnostics at Department of Semiconductor Optoelectronics, Institute of Materials Science and Applied Research, Vilnius University, Sauletekio Ave. 9- 3, LT-10222 Vilnius, Lithuania

* Corresponding author: Kestutis.Jarasiunas@ff.vu.lt

SiC and III-nitride power devices are promising for versatile applications in electronics and optoelectronics, ranging from high-frequency power controllers, switches, converters to high-power LEDs for projection displays, automotive headlights, and general lighting. These devices require high injection currents which translate into high current densities on the order of 100–1000 $A.cm^{-2}$. Consequently, together with development of advanced growth technologies, a relevant attention must be paid to investigation of recombination and transport processes at high carrier injection and for predicting an operation of power devices before their fabrication .

In this presentation we demonstrate applicability of nonlinear optical techniques for contactless monitoring of high density carrier plasma dynamics in wide bandgap semiconductors. The applied free-carrier grating (FCG) and free-carrier absorption (FCA) techniques are based on carrier injection by a short laser pulse and monitoring the spatial and/or temporal excess carrier redistribution via probe beam absorption or diffraction.

Light-interference pattern of two picosecond (ps) duration laser pulses (τ_L = 25 ps) at wavelength above the bandgap (355 nm for GaN, SiC and 213 nm for diamonds) was used for interband carrier excitation. This resulted in a spatial modulation of free carrier density $N(x) = N_0 + \Delta N\ (1+ \cos\ (2\pi x\ /\Lambda))$ and recording of a transient free carrier grating with a varying period Λ = 2 –20 μm. Strong absorption of light created carriers with density $\Delta N = 10^{18}$ -10^{20} cm^{-3} in a photoexcited layer which thickness from 1-10 μm (for GaN and diamond) up to 5-50 μm (for 3C or 4H SiC). Carrier recombination and lateral diffusion processes were monitored by a weakly absorbed ps probe beam, i.e. below the E_g (usually at 1064 nm). For measurements of FCA kinetics, a single pump beam was used for excitation, and the absorption kinetics were monitored by the optically delayed ps beam or by electronically delayed (up to 10μs) a 10-ns duration beam. The relationships between the measured optical signals and instantaneous carrier density ΔN (diffraction efficiency $\eta(t) = I_1/I_T \propto \Delta N(t)^2$ or differential transmission $\Delta T(t)/T_0 \propto \Delta N(t)$) provided straightforward determination of carrier lifetime τ_R and diffusion coefficient D.

At high excitation conditions, processes of nonlinear recombination and diffusion will lead to faster excess carrier dynamics, which is described by the following balance equation:

$$\frac{\partial \Delta N(x,t)}{\partial t} = D_a(N)\frac{\partial^2 \Delta N(x,t)}{\partial x^2} - \frac{\Delta N(x,t)}{\tau_R} - B\Delta N(x,t)^2 - C\Delta N(x,t)^3 + G(x,t)$$

(here B, C are the bimolecular and Auger recombination coefficients, and $G(x, t) = \alpha \cdot I(x, t)$ is the carrier generation function). In order to investigate carrier-density dependent processes, the rate of intrinsic nonlinear process must be higher or comparable with defect-related linear one. By ps-FCG technique we determined rates of recombination processes in GaN, SiC, InN, and diamonds. In GaN heterostructures, grown on different substrates (Si, SiC, or sapphire), nonradiative recombination τ_{NonRad} lifetime values from ≤100ps to ~3ns were found being inversely dependent on dislocation density in range10^8 to 10^{10} cm^{-2} [1]. In less defective MOCVD layers and free-standing HVPE films, the decreasing with excitation an average recombina-tion rate $1/\tau_R = 1/\tau_{NonRad} + 1/\tau_{Rad}$ confirmed a contribution of nonlinear (bimolecular) carrier recombination $\tau_{Rad} = 1/BN$ and the B= 2×10^{-11} cm^{-3}/s value. In 10^{18} to 5 $\times10^{19}$ cm^{-3} excess carrier denisty range, we measured both the decreasing with excitation carrier lifetime (from 3.8 ns to 1.3 ns) and the increasing D value (from 1.5 to 4.1 cm^2/s) at 300K in HVPE layer [2] (Fig. 1). Moreover, we observed ultrafast processes of stimulated recombination, both in InGaN and GaN heterostructures, while Auger recombination was not seen even at 10^{20} cm^{-3} carrier density. On the other hand, in bulk GaN crystals with high density of point defects we observed the opposite behaviour, i.e. the increasing with excitation carrier lifetime, from 0.9 ns to 3.1 ns [3], and attributed this effect to saturation of carrier trapping centers.

The current high-pressure high-temperature growth of diamonds provides 1 mm thick "nitrogen-free" crystals $N_N < 10^{17}$ cm^{-3}). The values of $\tau_R = 2.8$ ns and D = 9 cm^2/s have been measured [4] in type IIa high quality crystal at high excitations ($\Delta N = 5\times10^{18}$ cm^{-3}). These data provided bipolar carrier mobility of 360 $cm^2/V.s$ and diffusion length L_D= 1.6 μm. Never-theless, shorter carrier lifetimes at lower carrier density ($\sim10^{17}$ cm^{-3}) indicated presence of trapping centers, which became saturated at high excitation conditions. Similarly, the CVD diamond films provided τ_R = 0.6 ns values and L_D=0.5 μm, therefore investigation of pure intrinsic nonlinear effects in diamonds is hindered by the current stage of growth technology.

In 4H SiC, photoluminescence decay in thick epitaxial layers allowed to correlate variation of low-injection minority carrier lifetimes with density of lifetime-limiting deep defects Z1/Z2 [5]. This model was extended to high injection case, thus at conditions of trap saturation ($\Delta N = 10^{17}$-10^{18} cm^{-3}) the electron and hole lifetimes increased and became equal to $\tau_{R\ FCA} \approx 600$ ns at [5]. At even higher injections, FCA kinetics exhibited the decreasing with excitation lifetimes (τ_R <100 ns), and provided coefficients C = 7×10^{-31} cm^{-6}/s and B = 2×10^{-12} cm^{-3}/s [6]. Our study of FCA kinetics in bulk 3C (grown on undulant Si) provided linear lifetimes of ~53 ns from and their decrease down to ~10 ns at ~5 $\times10^{19}$ cm^{-3} (Fig. 2). The values of C ≈ 2×10^{-32} cm^{-6}/s and D ≈2.8 cm^2/s were derived at RT for bulk 3C. In sublimation grown 3C epilyers, lifetime and D values increased at carrier densities above 10^{18} cm^{-3}.

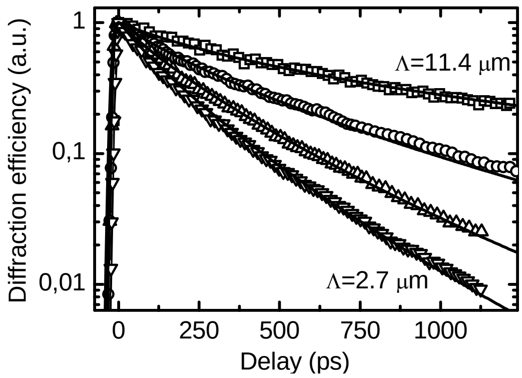

Fig. 1: FCG kinetics in HVPE GaN at different grating periods Λ (2.7, 3.2, 4.3, and 11.4 μm): experimental data (points) and modelling, using B=2×10^{-11} cm^{-3}/s value and $D = D_0(1+N/N_0)$ dependence with N_0 = 2×10^{19} cm^{-3}. Excitation density I = 2.7 mJ/cm^2.

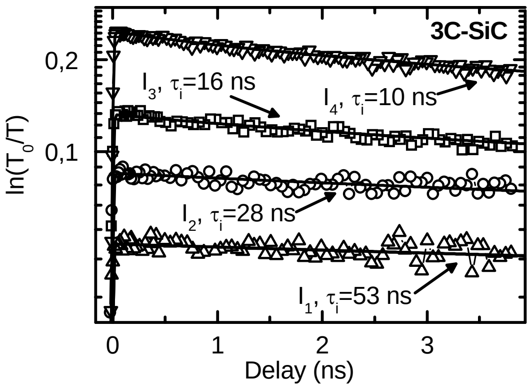

Fig. 2: FCA kinetics in bulk 3C-SiC at different excitations I (I_1-I_4 correspond to 6.6, 14.7, 24.4, and 33.0 mJ/cm^2): experimental data (points) and modelling (lines), which provided Auger coefficient value C ≈ 2×10^{-32} cm^{-6} s^{-1}.

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Application of SIMS and SNMS to mixed matrix semiconductor materials.

G.A.Cooke*
Hiden Analytical Ltd. 420 Europa Boulevard, Warrington, WA1 4EZ, UK
* Corresponding author: gcooke@hiden.co.uk

The development of secondary ion mass spectrometry has been closely linked to that of the semiconductor industry with SIMS being one of the few metrology tools able to detect dopant (both active and inactive) at junction level concentrations as well as contaminant species. One of the main reasons for the success of SIMS in this role is the relative ease with which quantification of dilute impurities can be made in a uniform matrix, a situation historically encountered in semiconductor devices. However, shrinking device dimensions and the use of varying semiconductor alloys presents new challenges [1]. This is especially the case with thin and graded complex matrices where changes in the ion yield can have a profound impact on the measured signal.

This paper discusses the application of SIMS to semiconductor metrology, including the use of low energies for high depth resolution [2] and finely focussed ion beams for high lateral resolution (FIB-SIMS) and assesses the factors necessary for a successful measurement in terms of detection limit, spacial resolution and quantifiability. A major limitation in quantitative SIMS is the requirement for a uniform matrix and a method has been developed for quantification in complex matrices by using simultaneous SIMS and SNMS (sputtered neutral mass spectrometry).

During SIMS analysis the sample is bombarded by a primary ion beam with an energy of between 200 eV and 30 keV causing sputtering of the surface. A fraction of the sputtered material is ejected in an ionised state and this is electrostatically directed into a mass spectrometer where it is detected using a pulse counting system. Thus the composition may be determined. It is generally the case that primary ions with lower bombardment energies penetrate less deeply and cause less damage to the sample, permitting better depth resolution. Finely focussed beams typically require higher bombardment energies to maintain the beam profile. Monitoring species as a function of sputter time permits a depth profile to be recorded.

The measured ion signal for a material, $\boldsymbol{i}$, is described by,

$$\boldsymbol{I_i = I_p\, c_i\, Y\, P_i\, T} \qquad (eq\ 1)$$

Where $\boldsymbol{I_p}$ and $\boldsymbol{I_i}$ are the primary and secondary ion currents respectively, $\boldsymbol{c_i}$ is the fractional concentration of i, $\boldsymbol{Y}$ the sputter yield, $\boldsymbol{P_i}$ the ionization probability and $\boldsymbol{T}$ the instrument transmission. Thus, in order for the measured signal to vary linearly with the concentration, $\boldsymbol{I_p}$, $\boldsymbol{Y}$, $\boldsymbol{P_i}$ and $\boldsymbol{T}$ must remain constant. When this is the case, quantification can be made by comparing the signals from a known amount of impurity with that of an unknown. Ion implantation provides a means to produce a wide variety of such reference materials, not only for semiconductors but also for a range of other applications. Unfortunately, the ionisation probability $\boldsymbol{P_i}$ varies significantly with material composition (often over orders of magnitude) leading to the requirement for uniform matrices and comparison with reference materials of near identical composition. Furthermore, when $\boldsymbol{c_i}$ becomes greater than a few percent, its presence can directly affect $\boldsymbol{Pi}$. It is important to note that typically $\boldsymbol{P_i}$ is much less than 1%.

This *matrix effect*, [3] presents significant difficulties when analysing dopants or contaminants in materials where the matrix changes. In layered structures, where the changes are abrupt, each layer may be treated independently, however, in the case of graded structures this is not possible. Unfortunately, graded alloys and mixed matrix materials are becoming more prevalent in the semiconductor industry, and, at the same time, the tolerance on the required accuracy is being reduced. Such materials are found in dielectrics, diffusion barriers and the semiconductors themselves, including non-dilute concentrations and precipitates in ultra shallow implants.

The most common method of quantifying the concentration scale of depth profiles is the use of the relative sensitivity factor (RSF) where the sensitivity of the instrument to the impurity is related to that of the matrix, this also corrects for any variation in the primary ion current $\boldsymbol{I_p}$ (which is usually not significant with modern instrumentation). The depth scale of an analysis is quantified by measuring the terminal depth of the measurement crater and assuming a uniform erosion rate in uniform materials. Again, layered structures with abrupt interfaces may be treated in a piecewise fashion by applying separate erosion rates to each layer.

In the case of graded structures, a series of reference samples may be produced such that the RSF can be determined as a function of alloy composition, enabling the correct *instantaneous* RSF to be applied at each point in the depth profile – *providing that the matrix composition at that point is known.* Unfortunately, the matrix effect generally prevents the use of SIMS to determine the matrix composition!

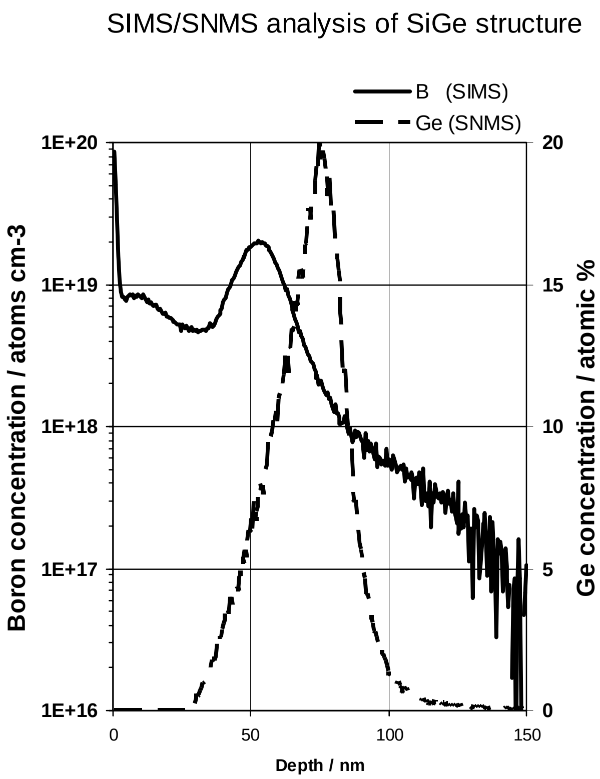
Sputtered neutral mass spectrometry, SNMS, uses very similar instrumentation to that of SIMS and can produce localised depth profiles in the same way. The crucial difference is that instead of relying on ionisation occurring at the time of sputtering, neutral particles are ionised *after* emission, by either electron impact [4], laser [5] or electron gas plasma devices [6]. The separating of the sputtering and ionizing events means that the matrix effect is all but removed, thus, in equation (1), $\boldsymbol{I_i}$ becomes proportional to $\boldsymbol{c_i}$ across the entire concentration range. However, although the ionisation probability is near constant, it is generally very small, meaning that SNMS detection is limited to the range 0.01% - 100%.

The Hiden MAXIM secondary ion mass spectrometer (fitted to the Hiden SIMS Workstation instrument) is able to switch between both SIMS and electron impact SNMS detection in a few hundred milliseconds. By combining SIMS, for sensitivity, with SNMS, for matrix quantification, within the same depth profile, the instantaneous matrix composition may be determined. Once this is done, the correct RSF may be applied to accurately quantify the impurity (dopant) at each point in the profile.

This scheme is highly applicable to semiconductors as the wide variety of growth techniques available and limited elements used, together with accurate ion implantation, means that reference materials are relatively easily manufactured.

It should be noted that the sputter yield, $\boldsymbol{Y}$, also varies as a function of matrix composition and a change in $\boldsymbol{Y}$ will be reflected in the measured signal $\boldsymbol{I_i}$, however, the change will affect all signals in a similar way, thus the change in the sum of the signals from the sample will directly reflect the erosion rate [7]. This effect may be used to dynamically characterise the erosion rate, alternatively, of the relative erosion rates of the reference samples are known, these may be applied on a point by point basis.

The plot below shows a quasi-simultaneous combined SIMS and SNMS analysis of a boron doped SiGe test structure. Analysis was undertaken using 5 keV O_2^+ primary ions bombarding at 45°. These conditions are designed to provide good sensitivity for detection of boron as the presence of oxygen significantly enhances the ionization probability for electropositive elements (often by orders of magnitude). During SNMS measurements, ions from the sample are deflected from the detection path by a lateral electric field. Neutral particles then traverse an electron impact ionization cell where ionization occurs. Ions are also created from the residual gas but these are filtered by virtue of their lower kinetic energy. After detection of neutral species, the bias on the filament supplying electrons to the ionizer is removed (preventing electrons from filling the cell), as is the lateral deflection field. Ions created by sputtering are then able to enter the spectrometer and sensitive SIMS detection is made. The linear calibration of concentration in SNMS mode requires only one reference point to be obtained in order to calibrate the entire concentration range. Indeed, this does not even have to be collected from a SiGe matrix, but can be from any Ge containing material. The fact that SNMS does not require the use of matrix matched reference materials which is of great benefit when the impurity concentration range spans both the SIMS and SNMS detection range as SNMS may provide calibration for SIMS.



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Physical analysis of Si-on-SiC by direct wafer bonding

M.R. Jennings[1], A. Pérez-Tomás[1], O.J. Guy[2], M. Lodzinski[2], P. Gammon[1], S. Burrows[1], J.A. Covington[1], P.A. Mawby[1]
[1]*School of Engineering and Physics Dept., University of Warwick, Coventry, CV4 7AL (UK)*
[2]*School of Engineering, University of Wales, Swansea, SA2 8PP (UK)*
[*] Corresponding author: M.R.Jennings@warwick.ac.uk

This paper presents an innovative approach to the fabrication of Si/SiC heterojunctions in the form of wafer bonding. The layer transfer of a silicon wafer onto SiC on- and off-axis substrates has been demonstrated utilising the *smartcut®* process. Physical examination techniques demonstrate a smooth topology suitable for device fabrication together with an abrupt interface.

SiC is the most promising of the wide bandgap semiconductors as a replacement for silicon for high power semiconductor devices [1]. The potential benefits exhibited by SiC are due to factors such as its technological maturity and native thermal oxide (SiO_2) with respect to other wide bandgap semiconductors such as gallium nitride and diamond. However, the lack of a high voltage semiconductor switching device is currently limiting the widespread uptake of the technology. It should be noted that SiC technology has the capability of delivering much higher efficiency power electronic systems [2]. SiC MOSFETs have traditionally suffered from high on-state losses due to poor channel mobilities underneath the gate oxide [3]. Here, we physically investigate a Si-on-SiC direct wafer bonding technique based on the *smartcut®* process for the purpose of defining a reliable, carbon-free gate oxide. It should also be noted that this technology could allow the monolithic integration of both Si and SiC devices on the same chip. Here, the intelligent CMOS circuitry would be implemented in well-defined silicon processes, while the power device would be fabricated in SiC. Another application of such structures include novel Si/SiC heterojunction MOSFET fabrication with the channel region implemented in silicon and the blocking capability being realised within the SiC.

Commercial 3" on- and off-axis SiC substrates doped at 10^{16}-10^{17} cm^{-3} respectively from Cree Inc., USA were utilised for the wafer bonding process. 4H-SiC epitaxial layers are 3.92° off-axis while on-axis substrates have a 0.08° orientation. The smartcut process transferred a 400 nm thick p-type silicon wafer doped at 1.0×10^{17} cm^{3} at room temperature. The wafer bonding process is highlighted in figure 1. Prior to wafer bonding the silicon wafer was implanted with H^+ ions with an energy of ~200 keV, with a dosage of 10^{16}-10^{17} cm^{-2}. Wafer cleaning was then performed utilising an oxygen plasma treatment and standard cleaning (SC) procedures. After rinsing and drying, the wafers were bonded in an ultra high vacuum (UHV) at room temperature, followed by a 150 °C anneal for a sufficient cleaving bond strength to be achieved. Finally, cleaving was performed at 300 °C with a subsequent 1100 °C anneal (2 hours) for chemical bond strengthening. On-axis SiC wafers produced the highest quality wafer bonding due to smoother surfaces. SiC epitaxial layers are inherently rougher due to the "terrace" arrangement of silicon and SiC atoms at the surface. We presume that root a mean square (rms) roughness of <0.5 nm is required for successful layer transfer to be achieved.

Next, the wafer bonded structure was physically analysed with the aid of a scanning electron microscope (SEM), specifically, the examination of the cross-section. The cross-sectional SEM image of the on-axis Si/SiC heterojunction structure is shown in figure 2. From figure 2, it can be inferred that the interface at the Si/SiC heterojunction is abrupt, exhibiting no evidence of any defects that extend into the silicon layer. The abruptness of the Si/SiC heterojunction bodes well for future electrical characterisation and power device fabrication. The topology of the wafer was examined utilising atomic force microscopy (AFM). An AFM image of the on-axis Si/SiC heterojunction structure is shown in figure 3. We have previously

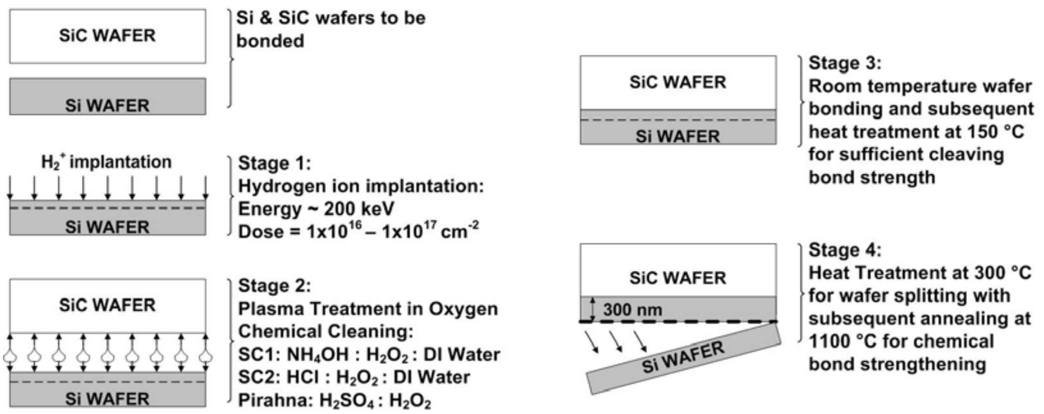

Fig. 1: Summary of the Si/SiC wafer bonding process undertaken in this work.

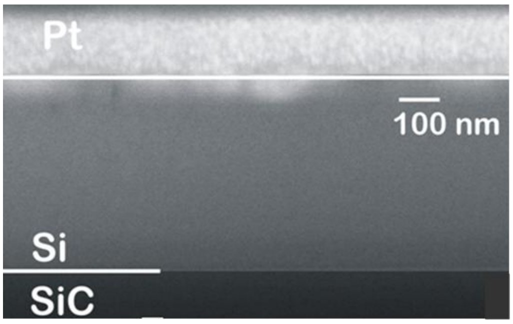

Fig. 2: SEM image showing cross-section of the Si/SiC heterojunction structure.

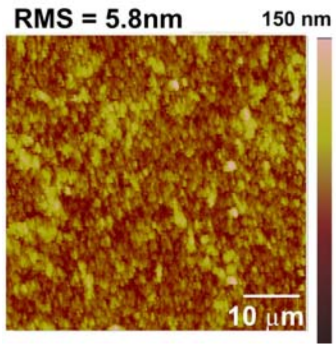

Fig. 3: AFM image showing surface topology of Si/SiC heterojunction structure.

reported on the formation of Si/SiC heterojunctions with the use of molecular beam epitaxy (MBE) silicon deposition [4, 5]. These structures yielded rms roughness values as high as 210 nm, which is completely unacceptable for semiconductor device fabrication. In contrast, wafer bonding Si/SiC heterojunction structures demonstrate rms roughness values in the region of 5.8 nm, shown in figure 3.

In summary, we have presented a physical analysis of Si/SiC heterojunctions fabricated by direct wafer bonding. The physical analysis undertaken by SEM and AFM point to the fact that Si/SiC heterojunctions fabricated by direct wafer bonding display smooth surfaces and abrupt junctions. Applications include the consumption of the silicon for the realisation of stoichiometric, carbon-free SiO_2, novel heterojunction MOSFETs and the monolithic integration of silicon and SiC devices.

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Heteroepitaxy of 3C-SiC on different on-axis oriented Silicon substrates

R. Anzalone[1,2,*], A. Severino[1,2],G. D'Arrigo[1], C. Bongiorno[1], G. Abbondanza[3], G. Foti[1], S. Saddow[4] , F. La Via[1].

[1]CNR-IMM, Strada VIII n.5, Zona Industriale, 95121, Catania, Italy

[2]University of Catania, Phys. Dept., via Santa Sofia 64, 95125, Catania, Italy

[3]Epitaxial Technology Center, 16° Strada, Pantano D'Arci, Con.da Torre Allegra, 95030, Catania, Italy

[4]Dept. of Elect. Engineering, University of South Florida, E. Fowler Ave., Tampa, Florida, USA

* Corresponding author: ruggero.anzalone@imm.cnr.it

Silicon carbide (SiC) is considered to be a good candidate for power electronics due to its excellent properties such as wide band gap, high breakdown field, and high thermal conductivity [1]. Among the polytypes of SiC, cubic SiC (3C-SiC) possesses unique properties, such as high electron drift velocity, which is more suitable for high-frequency power devices [2]. The large lattice mismatch, which is about 20% (a_{SiC}=0.436 nm, a_{Si}=0.543 nm), is blamed for the generation of misfit dislocations and stacking faults at the interface, which has been limiting device development.

The hetero-epitaxy of 3C-SiC on Si, as expected, is strictly related to the orientation of the Si substrate used for the growth. In a diamond cubic crystal structure such as for Si, the atomic lattice packing density and the available bonds in the crystallographic plane are strongly related to the crystallographic orientation of the film.

One of the intentions of this work is to study the substrate orientation affect on SiC films.

The growth experiments were carried out by low pressure chemical vapour deposition at 1350°C, using trichlorosilane ($SiHCl_3$), ethylene (C_2H_4) and hydrogen (H_2) as the silicon supply, carbon supply and gas carrier, respectively. Chlorine addition is known to suppress the homogeneous nucleation of silicon droplets in the gas phase. In fact, the simple replacement of SiH_4 with $SiHCl_3$ (TCS) produces a significant alteration of the chemical species involved in the reaction, whose key factor is represented by the shift from Si to $SiCl_2$ as the most important silicon-containing precursor [3].

3C-SiC epitaxial films were then evaluated from X-Ray pole figures, recorded at the Bragg condition corresponding to $2\theta \approx 35.59°$, the angle corresponding to the (111) 3C-SiC planes. The pole figures were obtained by scanning the tilt angle χ and the azimuth rotation angle φ. To understand the results obtained we have used the CaRIne v.3.5 pc software to simulate the theoretical diffraction spot locations on the Ewald sphere of the (111) 3C-SiC pole figure. Figure 1 shows an XRD pole figure and the software simulation of the 3C–SiC film grown on a (100)-oriented Si substrate with 30 minutes growth process. The analysis shows four strong peaks at an angle of approximately 54.7 degree in χ. These four peaks correspond to the diffraction from the {111} 3C–SiC planes. Four other peaks crossing the (100) 3C–SiC pole at about 15.8 degree in χ were also observed. In figure 1 all of the peaks from the simulation (black circled spots) were added to the observed peaks. It turns out that these signals came from a twin of the {111} 3C-SiC plane. In this way we found out that the peaks referred to χ=15.8° resulted from a single twin of the pole at χ=54.7°. Therefore, we may safely conclude that these four weak peaks result from the twinned {111} 3C-SiC planes, suggesting the existence of a symmetrical twin band around the <111> axis.

The same technique can be applied to study the twin density of the (111) 3C-SiC films grown on (111) Si substrates. Figure 2 shows the presence of four strong peaks coming from {111} 3C-SiC planes, three of them being at χ=70,5° and one at χ=0°, corresponding to the film surface. Three groups of four low intensity poles with a rhombohedra shape, observed at about χ=37.5°, χ=55.5°, χ=56° and χ=69.5°, have been detected as well. The numerical simulation allowed us to reproduce all of the signals of the pole figure. We found out that these low intensity peaks were related to first order twins of the {111} 3C-SiC planes, since each regular pole twinning results in three low intensity peaks. In figure 3 is shown a pole figure referred to 3C-SiC grown on Si(110) oriented and the software simulation. From the θ–2θ XRD scan analysis (not shown) was observed that by growing on the (110) Si orientation the 3C-SiC epitaxial growth direction was along the <111> direction and not along <110> as one would have expected. The pole figure shows that the {111} 3C-SiC plane-related pole is at the centre of the circumference. At the same time it is possible to observe the presence of many intense peaks that are not expected when observing the crystal from the <111> or <110> directions. To understand these results we have used the CaRIne v.3.1 software to simulate the pole figure peak positions. We have started the simulation with the crystal oriented along the <110> 3C-SiC direction. This starting configuration shows two poles at $\chi=34.7°$ and four at $\chi=90°$ related to the {111} planes. By simulating the possible crystal twinning around these poles up to second order, it turned out that the <111> direction of the 3C-SiC crystal was not aligned to the <110> Si direction. From the simulation we see that the (111) pole is shifted by 3.5° along the <002> Si direction. For this reason we set a misalignment of 3.5° between the {110} 3C-SiC plane and the {110} Si plane along the <002> Si direction. With these new parameters we were able to reproduce all the poles in the polar figure with the 3C-SiC (111) plane parallel to the surface. At the same time, we have found a more intense pole referred to the 3C-SiC <115> orientation, parallel to the Si <110> direction and their corresponding twins. With the simulation we also discovered that a translation from the center of 3.5° along the <002> Si direction makes more probable the detection of twins on one pole than on the other. The presence of tails in a pole at χ=34.7° (fig. 2) is the evidence of this situation [4]. In addition to the fact that different orientations used for the hetero-epitaxy affect the crystalline quality of 3C-SiC this is also clearly underlined by the evaluation of the residual average stress of the SiC/Si system performed by measuring its curvature radius. The curvature was deduced from surface profile measurements made along a line. The trend of the average residual stress, from the modify Stoney equation, of 3C-SiC on Si(100), Si(110) and Si(111) as a function of the thickness is shown in figure 4. From this further comparison it is possible to observe how the different substrates drastically affect the average stress inside the film.

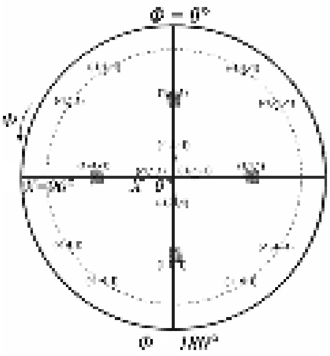

Fig. 1: X-Ray pole figure of 3C-SiC on Si(100) oriented

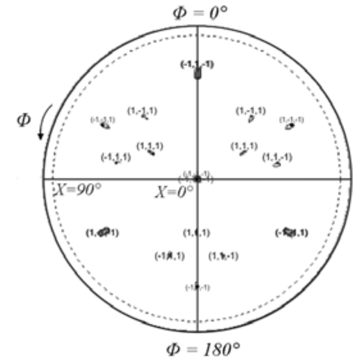

Fig. 2: X-Ray pole figure of 3C-SiC on Si(111) oriented

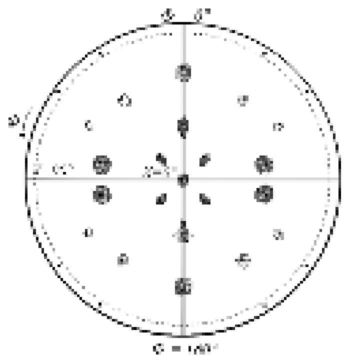

Fig. 3: X-Ray pole figure of 3C-SiC on Si(100) oriented

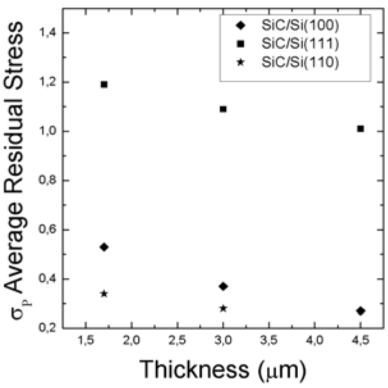

Fig. 4: Radius of curvature stress measurement as a function of thickness performed on 3C-SiC film grown on different Si substrate.

All the performed analysis on the samples proved as the Silicon substrate orientation strongly affects the Silicon Carbide crystallographic proprieties.

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Growth and characterization of β−SiC and β−SiC/SiO_2 core-shell nanowires

G.Attolini*, F.Rossi, M.Bosi, B.E.Watts, F. Fabbri, G.Salviati
IMEM-CNR Institute, Parco Area delle Scienze 37/A, 43100 Parma (Italy)
* Corresponding author: giovanni@imem.cnr.it

The combination of the distinctive physical and chemical properties of SiC and unique advantages of nanowires (NWs) opens promising near-future perspectives for the design and fabrication of nano-scale devices. The main interests are addressed to nanoelectronic devices (e.g. nano field-effect transistors) and nano-electromechanical systems able to operate even in harsh environments, and to nano-sensors exploiting the SiC NWs as biocompatible nanoprobes for biological systems.

β−SiC and β−SiC / SiO_2 core-shell nanowires have been prepared on silicon substrate by using carbontetrachloride and carbon monoxide respectively.

β−SiC (without core-shell) NWs were obtained through a chemical reaction in which carbontetrachloride (CCl_4) acted as a precursor. By this method the decomposition of CCl_4 produces chlorine which, by reacting with silicon, gives rise to silicon chlorides that recombine with carbon to yield silicon carbide. The reaction takes place in a quartz open tube under a flow of nitrogen at a temperature range of 1273-1373 K [1].

β−SiC/SiO_2 core-shell NWs have been prepared with carbon oxide and nickel as catalyst in nitrogen atmosphere at the temperature between 1323 to 1373 K [2].

In secondary electron images it is possible to see that the β−SiC NWs form a dense network of high quality, long, interwoven fibres (Fig.1 a), while the core/shell NWs are vertically aligned (Fig. 1b). Both the samples show several hundred microns long NWs and have uniform diameters below 40 nm.

The nanowires crystalline structure were analysed by X-ray diffraction on a Siemens D500 diffractometer with a Cu Kα radiation. For both samples XRD patterns confirmed the characteristic peaks at 2θ =35.6° (111), 41.4° (200), 59.9° (220), 75.5° (222) indexed as β−SiC.

The detailed NWs lattice structures was investigated by Transmission Electron Microscopy (TEM), with a field emission JEOL 2200 FS instrument operating at 200kV.

The core has a cubic structure with some stacking faults and rotational twins mainly on (111) planes perpendicular to the growth axis, as common in β-SiC. The SFs can originate very local segments of different polytypes (e.g. 2H, 4H, 6H) (Fig 2a).

The core shell structure consists of a SiC core enveloped by evident amorphous silicon oxide (Fig. 2b).

Future experiments will be aimed to study the applications of the oxidised NWs as cylindrical nano FETs and as electro-optical chemical sensors and of the pure SiC fibers as nanoprobes functionalised with specific organic molecules (e.g. porphyrins) for a new-class of biosensors based on molecular recognition. The choice of porphyrins to create a suitable inorganic/organic system is also supported by a good match between the green optical emission of the SiC NWs and the porphyrin absorption Q band. This could allow an efficient inorganic/organic energy transfer, exploitable for instance to realize electro-optical sensing devices.

a) b)

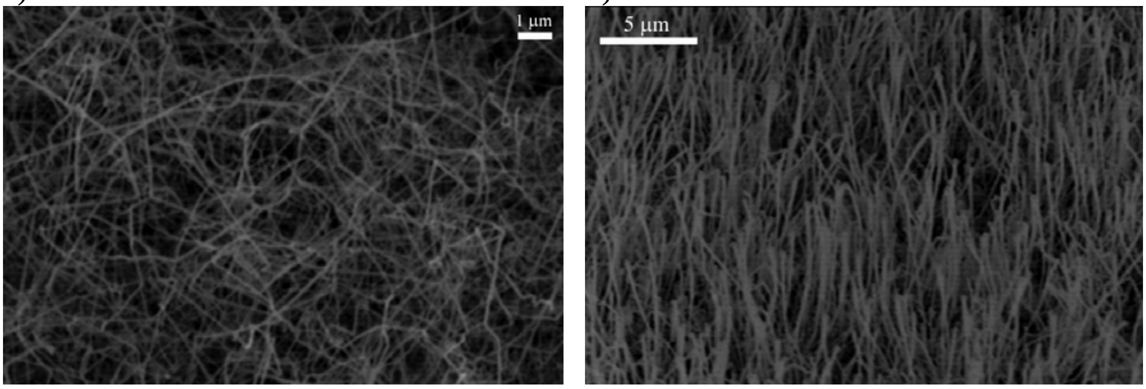

Fig. 1: SEM image of 3C-SiC wires, a) pure nanowires, b) core-shell nanowires

a) b)

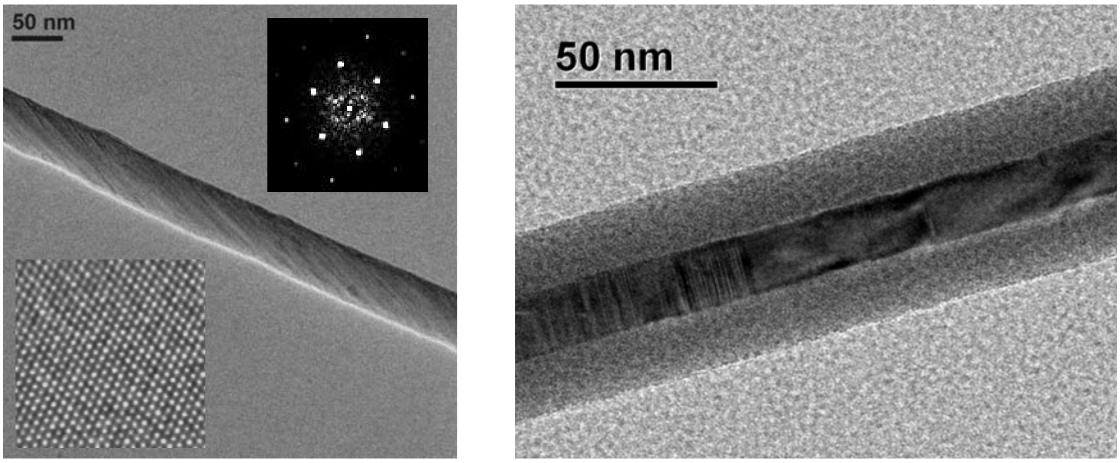

Fig. 2: TEM images of a typical β-SiC NW (a) and a typical β–SiC / SiO_2 core/shell NW (b). A high resolution image of a perfect region and the corresponding diffractogram are shown as inset in (a).

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Influence of defect density on the Schottky barrier height on a 3C/4H-SiC heterostructure

M.H. Weng[1*], J. Eriksson[1, 2], F. Roccaforte[1], F. Giannazzo[1], S. Di Franco[1], C. Bongiorno[1], S. Leone[3], V. Raineri[1]
[1] *CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy*
[2] *Scuola Superiore - Università di Catania, Via San Nullo 5/i, 95123, Catania, Italy*
[3] *Department of Physics, Chemistry and Biology, Linköping University, Sweden*
[*] Corresponding author: minghung.weng@imm.cnr.it

Silicon Carbide (SiC) based field effect devices over the last few years have been studied extensively with improvements in process engineering and wafer growth technology. Developments in epitaxial growth have demonstrated the possibility of forming heterojunction structures, where the polytype of silicon carbide merges, for example 3C-SiC (cubic) on 4H-SiC (hexagonal or α-SiC) substrates. One of the key issues currently limiting the performance of such SiC heterostructure devices is that of defects due to growth, i.e. lattice mismatch, particularly in 3C-SiC.
Exempted from huge lattice mismatch (20%) and expansion coefficient mismatch (8%, at temperature 475K) of 3C-SiC growing on silicon, 3C/α-SiC only encounters less than 0.1% lattice mismatch on the growth plane. In our study, research grade 4H-SiC on-axis substrates were used to grow the heterostructures. The 3C-SiC epitaxial growths were conducted in a horizontal hot-wall reactor at a pressure of 100 mbar, with hydrogen as carrier gas [1]. Vertical Schottky structures were fabricated on circular Au contacts of 100nm thickness, ranging from 5 to 150 μm in radius. The micro- and nano-electrical characteristics were acquired using a Karl Süss probe station, equipped with a parameter analyzer, and a Veeco DI dimension 3100 equipped with the conductive module, respectively.
Defects were characterized by electro-structural measurement, where conductive Atomic Force Microscopy (C-AFM) reflects a highly conducting behavior in the proximity of defects (for example, stacking faults, SF) in the current map. Defective lines/areas found in the current map are used to determine the defect density, *D*, for a given contact area. Figure 1 shows electrical currents (in the insert), which are corresponding to structural SF, and the defect density is found to be 1.8×10^{6} cm^{-2}. Figure 2 shows a planar image of the investigated sample where extended defects are visible. Double positioning boundaries (DPB) are identified where boundaries from different domains meet on the growth plane. In addition, stacking faults are further investigated by transmission electron microscopy, which reveals that such defects originate from the 3C/4H interface and propagate to the surface. For large contacts, with radius between 50 and 150 μm, conventional current-voltage (I-V) measurements were carried out. Smaller Schottky diodes (i.e. radius from 5 to 20 μm) could be characterized by means of the biased conductive diamond tip. From the I-V curves measured by C-AFM, the threshold voltage at which the diode is brought into a conducting state was extracted. This value is directly related to the Schottky barrier height as extracted by thermionic emission theory in microscopic measurements. From Murphy's formula [2], the theoretical yield, Y_D, is given by $Y_D = [1 - exp(-DA)]^2 / (DA)^2$, where *D* is the defect density, and *A* is the area. Figure 3 shows extracted and fitted values, where theoretical barrier heights are calculated with consideration to defect density and yields using the above equation. Both barrier heights obtained from electrical measurements and modeled ones follow a similar trend, i.e. an increase of barrier height with a decrease of the area. Our analysis allowed demonstrating that the electrical property of the diodes is strictly influenced by the presence of defects in the defined areas.

A novel approach to study the influence of defects on the barrier height of Schottky contacts is presented. We investigated electrical properties of vertical Au Schottky diodes as a function of material quality and contact geometry on heteroepitaxially grown 3C-SiC on 4H-SiC. In conclusion, the finding of the better behavior of diodes with smaller contact area on 3C-SiC significantly improves Schottky diode properties on cubic SiC, and it could establish wider acceptance in the selection of use of this polytype or heterostructure in silicon carbide technology.

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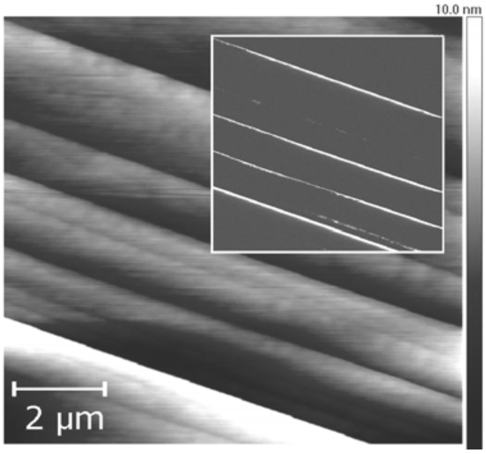

Fig. 1: Morphology taken by C-AFM. Insert shows corresponding current map in the same scan area, where bright lines measure leakage current in excess of 1 pA.

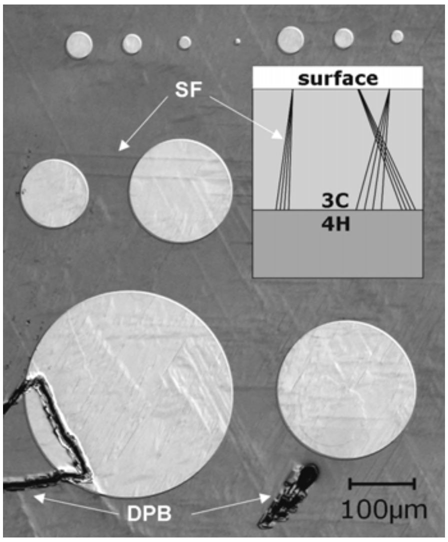

Fig. 2: Optical image showing possible SF and DPB defects on the diodes. Cross-section drawing illustrates SF originating from interface to surface.

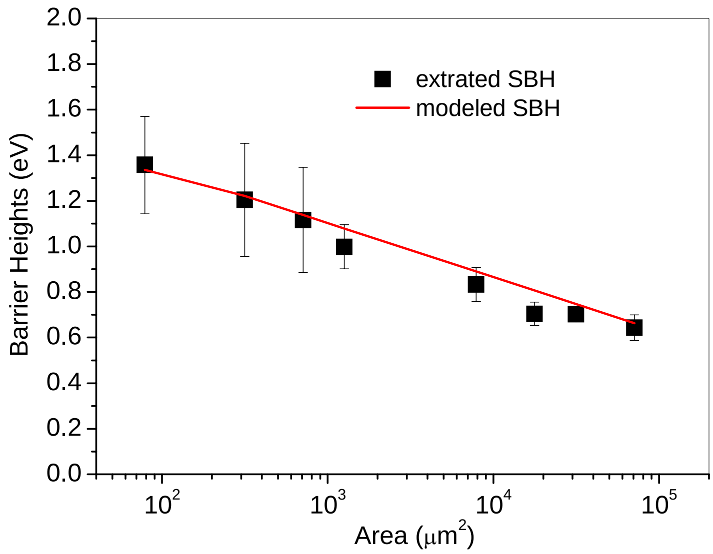

Fig. 3: Schottky Barrier Heights (SBH) versus area of the diodes. The continuous line is a fit to the model.

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Electrical transport properties of catalyst-free grown 3C-SiC nanowires

K. Rogdakis[1,2*], E. Bano[1], L. Montes[1], M. Bechelany[3], D. Cornu[4], K. Zekentes[2]
[1]IMEP-LAHC/INPG , MINATEC, 3 parvis Louis Neel-BP 257, 38016 Grenoble Cedex 01, France
[2]MRG-IESL/ FORTH, Vassilika Vouton, Greece
[3]LMI-UMR 5615 CNRS, Université Lyon 1, 43 bd du 11 novembre 1918, F-69622 Villeurbanne Cedex, France
[4]IEM UMR 5635 CNRS, ENSCM, Université Montpellier 2, CC047, 2 place Eugène Bataillon, F-34095 Montpellier cedex 5, France
[*] Corresponding author: rogdakik@minatec.inpg.fr

Back-gated field effect transistors (FETs) based on catalyst-free grown 3C-SiC nanowires (NWs) were fabricated and electrical characterization is presented. Silvaco simulation was used to fit the I-V characteristics and extract information about the carriers (electrons) concentration and the oxide/NW interface quality. The high traps density and fixed charges at the nanowire/oxide interface, D_{it}~$5x10^{11}$ $cm^{-2}eV^{-1}$ and Q_f ~$3x10^{13}cm^{-2}$, and the high electrons concentration (~$3x10^{19}$ cm^{-3}) originating from unintentional doping severely affect the electrical conduction through the nanowires which has as a result low values of mobility and transconductance, 0.06 cm^2/Vs and $7x10^{-10}$ A/V, respectively.

Recently, one-dimension nanostructures have become the focus of intensive research owing to their unique applications in mesoscopic physics and fabrication of nanoscale devices [1, 2]. Because of their low density of electronic states, nanowires in the limit of small diameters are expected to exhibit significantly different optical, electrical and magnetic properties from their bulk 3D crystalline counterparts. Much effort has been done on the growth of 3C-SiC nanowires with small diameter, suitable for the development of a nanowire FET. There are few studies in bibliography on 3C-SiC nanowire FETs, to the time being, all presenting similar device performances in terms of transconductance and mobility [3-5]. In this work, 3C-SiC nanowires were grown in a conventional furnace without presence of catalyst using as solid precursors of Si and C, namely SiO (s) and polypropylene (PP), respectively [6]. A nanowire suspension in ethanol was prepared and droplets were dispersed over a highly doped n-type silicon substrate coated with 265 nm of thermal SiO_2 with predefined large Ti/Au metal pads. The Si substrate was served as a back gate. The position of the nanowires was imaged by AFM (Dimension III, Vecco). Using e-beam lithography (Jeol JSM-7401F) and lift off process, local Ni/Au (50/50 nm) contacts to nanowires were prepared as shown in Figure 1a. Ni was used due to the low contact resistance with 3C-SiC [7]. Prior to the metal deposition by e-beam evaporation, the native oxide on 3C-SiC NW was removed by buffered HF to avoid poor contacts between metal lines and 3C-SiC NWs. The back-gated nanowire-based field effect transistors (NWFETs) have channel length of 700 nm and nanowire diameter ~80 nm. Based on I_D-V_G characteristics (Figure 1b) the electron mobility was estimated from the transconductance, $g_m = \frac{dI}{dV_g} = m(\frac{C}{L^2})V_{sd}$, where μ is the carrier mobility, C is the gate capacitance and L is the length of the 3C-SiC NW. Although the real device capacitance is in the order of atto-Farad and is difficult to be experimentally measured, it can be estimated by an approximated cylinder to plate capacitance model which gives $C=2\pi\varepsilon\varepsilon_o L/\ln(2t_{ox}/r)$, where ε is the dielectric constant, t_{ox} is the thickness of the silicon oxide layer, r and L are the 3C-SiC NW radius (40 nm) and length (700 nm) respectively. The transconductance of 3C-SiC NWFET was computed as g_m=$7x10^{-10}$ A/V. Following this commonly used approximated method, the estimated experimental electron mobility was 0.06 cm^2/Vs. We fitted the above experimental results by using Silvaco simulation package

(Figure 1b) with error less than 2%. We obtained the best fitting when a) n-type doping of NWs is equal to $3x10^{19}$ cm^{-3}, b) electrons mobility value is equal to 0.66 cm^2/Vs , c) Q_f $\sim 3x10^{13}cm^{-2}$ and $D_{it}\sim 5x10^{11}cm^{-2}eV^{-1}$. It is known, that the cylinder to plate capacitance model overestimates the nanowire FET capacitance [8], which leads to an underestimation of mobility. This explains the small discrepancy between Silvaco simulated mobility and the experimentally extracted [5]. The device performance is severely affected from the high unintentionally n-type doping ($\sim 3x10^{19}$ cm^{-3}) and the high traps density and fixed charges at the nanowire/oxide interface. Rapid thermal annealing is expected to improve the performance.

Device fabrication and SEM analysis were accomplished in Platforme Technologique Amont (PTA), Grenoble, France. K.R would like to thank Dr G. Katsaros (INAC SPSMS LaTEQS, CEA/France) for his assistance on e-beam lithography process and Prof. S. K. Lee (NDSL, S. Korea) and his group members for fruitful discussions on device fabrication.

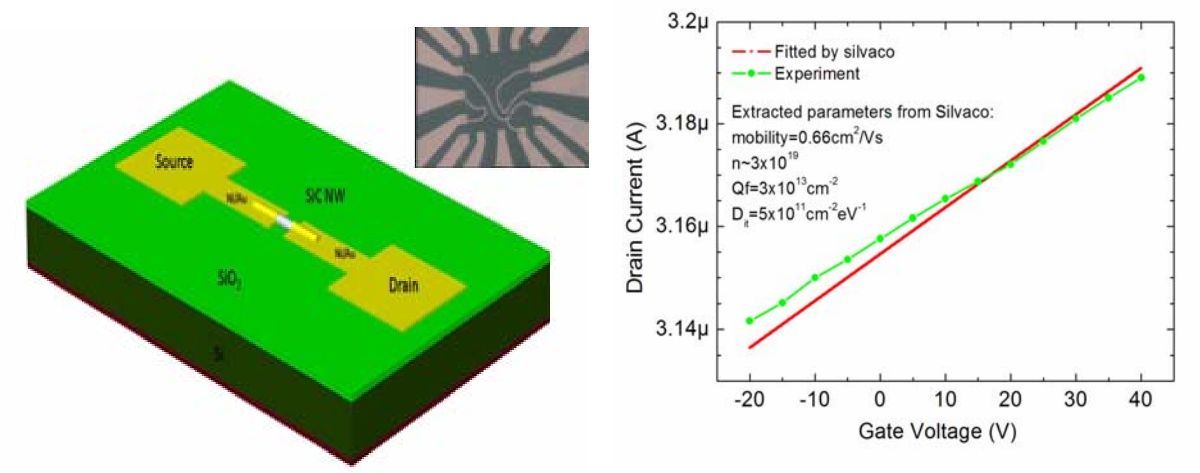

Fig. 1: (a) 3D device schematic view (inset: optical image of devices), b) experimental and fitted with Silvaco transfer characteristics of 3C-SiC NWFET

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On the structural defects and the polytype stabilization in LPE grown 6H-SiC layers

I. G. Galben-Sandulache[1*], F. Mercier[1], M. Marinova[2], D. Chaussende[1], E. K. Polychroniadis[2]
[1] *Laboratoire des Matériaux et du Génie Physique CNRS UMR 5628, Grenoble INP Minatec, BP 257, 38016 Grenoble Cedex 01, France*
[2] *Departement of Physics, Aristotle University of Thessaloniki, GR 54124 Thessaloniki, Greece*
[*] Corresponding author: irina.galben@grenoble-inp.fr

The growth of SiC from the liquid phase has long been studied as a promising growth method for obtaining micropipe-free wafers with low dislocation density [1]. Although encouraging studies have been reported this method remains a challenge from two points of view: the handling of the liquid silicon at high temperatures and the control of the growth front. These difficulties are directly related to the low C solubility in liquid silicon at temperatures below 1800°C [2].
In this work 6H-SiC homoepitaxial layers grown by a liquid phase epitaxy (LPE) method was studied. The method consists in a top seeded solution growth in which the C transport from the liquid to the seed surface is increased by the forced convection (rotation of crystal and/or crucible). On-axis 6H-SiC wafers were used as substrate. The solvent consisted in pure Si or Si+metal. The growth temperature was 1800°C. The grown layers were investigated by transmission electron microscopy (TEM). The influence of the substrate polarity, crucible geometry and the nature of the solvent is discussed regarding the crystalline quality of the grown layers and the defects appearing.
The growth on Si-face substrates favors the formation of stacking faults (SFs) with relatively high density in the grown layer, Fig. 1. The rotation of the crucible and/or the seed influences slightly the SF density over the layer thickness. Moreover, if Al is added to the solvent, the polytype stabilization becomes very difficult and occurrence of long period polytypes (like 27R-SiC, 69R-SiC and 108R-SiC) is observed. Fig. 2 shows part of the layer grown on Si face substrate using mixture of Si and Al as a solvent, where, as seen in the image, the formation of at least three different local sequences is obvious. On the other hand C-face substrates and usage of pure Si as solvent promote the formation of layers free of defects as shown in Fig. 3. The addition of Al obviously induced strain in the grown layers and leads to enhanced formation of dislocations in the near substrate/layer interface region (see Fig. 4).
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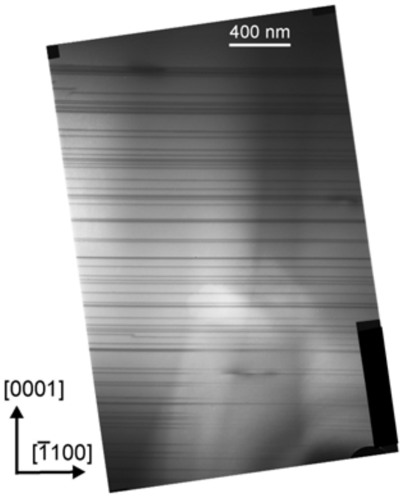

Fig. 1: A TEM micrograph, showing the relatively high SF density in the layers grown on the Si face substrates with pure Si used as a solvent.

Fig. 3: A TEM micrographs from the layer grown on C face 6H-SiC substrate using pure Si as a solvent.

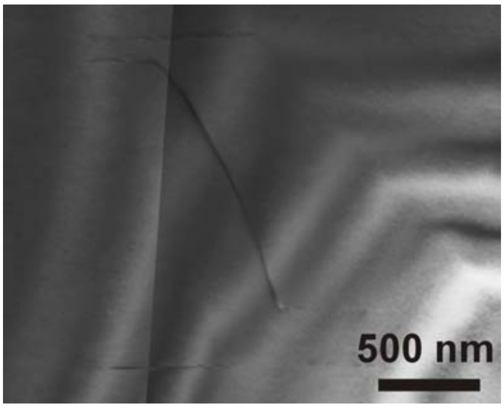

Fig. 4: A TEM image from the layer grown on C face 6H-SiC substrate using mixture of Si and Al as a solvent. It reveals the enhanced formation of dislocations in the near substrate /layer interface region.

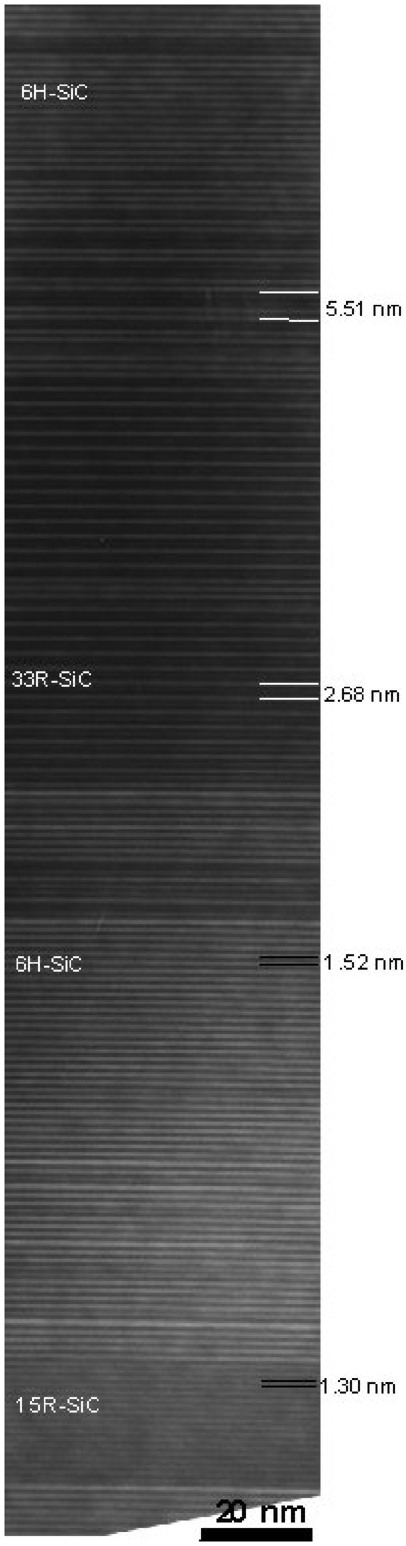

Fig 2: TEM micrograph of the layer grown on Si face substrate using a mixture of Si and Al as a solvent.

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The effect of different substrate preparations on growth of cubic silicon carbide

R. Vasiliauskas[1*], M. Syväjärvi[1], M. Beshkova[1], J. Lorenzzi[2], G. Ferro[2], R.Yakimova[1]
[1]*Department of Physics, Chemistry and Biology, Linkoping University, SE-581 83 Linköping, Sweden*
[2]*Laboratoire des Multimateriaux et Interfaces, UMR-CNRS 5615, UCB-Lyon1, 43 Bd du 11 nov. 1918, 69622 Villeurbanne, France*
* Corresponding author: remis@ifm.liu.se

In off-axis growth of hexagonal SiC, nucleation is determined by ledges of steps, thus homoepitaxial growth is achieved. On-axis surfaces are needed to form 3C-SiC. Nucleation is then critically dependent on growth conditions, and there will be competition between nucleation of 6H-SiC and 3C-SiC.
Growth of 3C-SiC was performed by sublimation epitaxy [1] on the Si-face of on-axis (0001) 6H-SiC substrates. All growth experiments were performed at identical conditions: growth temperature 1775^{o}C, growth time – 30 min and the temperature ramp-up - 5 K/min.
Four different substrate preparations were studied: (i) as received 6H-SiC substrate, (ii) re-polished by Novasic to minimize surface roughness; (iii) annealed and covered with thin Si layer [2]; (iv) with 1.5 μm 3C-SiC layer grown by VLS growth using Si–Ge melt [3].
In general, one can expect that the different surfaces affect growth and nucleation in different ways. More rough surfaces would then act as nucleations sites for 6H-SiC instead of favoring formation of 3C-SiC, and smoother surfaces would favor formation of more 3C-SiC centers as these are usually created by two-dimensional island formation on smooth surfaces [4], i.e. result in larger percentage of 3C-SiC on the substrates. However, there was no significant difference between growth on as-received and re-polished substrates. On both substrates coverage by 3C-SiC compared to 6H-SiC was ~ 87 %. Thus a smoother substrate surface does not influence much on 3C-SiC nucleation. Likely this observation suggests that as at the temperature ramp up there is initial homoepitaxial 6H-SiC growth, and this is very important for the 3C-SiC formation. Only when perfectly on-axis regions are formed the 3C-SiC nucleates [4, 5].
Growth on silicon covered substrates showed less nucleation of 3C-SiC as only about 45% was covered with 3C-SiC (Fig. 1b). One can argue that this is resulting from the excess of Si on the substrate surface (some Si droplets were observed after growth). It should enhance homoepitaxial growth as for liquid phase growth techniques. However, one has to bear in mind that the Si/C ratio at vapor phase growth below 2000^{o}C is already Si-rich and an increase of Si/C ratio generally increases the probability of 3C-SiC formation. On the other hand, the annealing is made to create steps, which favors 3C-SiC growth in VLS [2]. In the VLS growth the 3C-SiC starts to nucleate at the terraces of these steps. However, in vapor phase growth the steps enhance growth at the ledges, and reproduction of the substrate polytype, as observed by a lower percentage in 3C-SiC when using Si-covered substrates, which have been annealed.
Almost full 3C-SiC coverage was achieved on substrates with VLS grown 3C-SiC layer, having 99.9 % 3C-SiC in the layer grown by sublimation epitaxy. The polytype coverage on the four types of samples is collected in Figure 2. The delicate temperature ramp-up [6] is thus well suited with the 3C-SiC layer, and homoepitaxial growth occurs. The surface of the 3C-SiC layer was considerably improved compared to the VLS, which contains steps like typical in solution growth methods. These results are very promising, while work is needed to perfectly adapt the VLS layer influence on the sublimation epitaxy growth.
This work was supported by FP6 Marie Curie Action - Research and Training Network - MANSiC - contract N°035735.

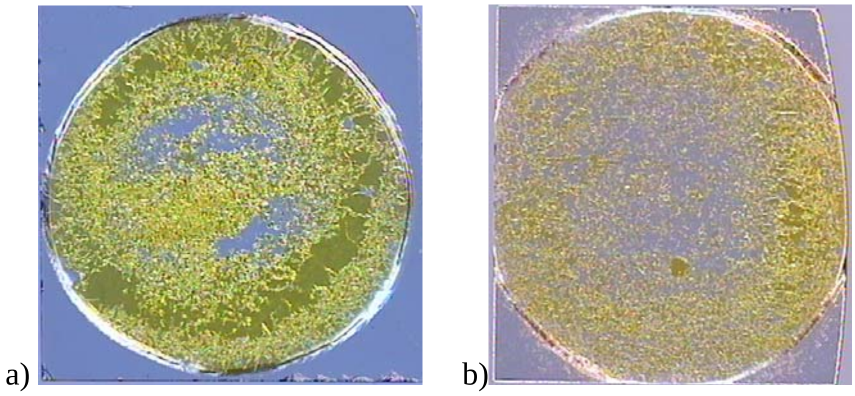

Fig. 1. (a) Image showing 87% of 3C-SiC in growth on as received substrates; (b) images showing 45% of 3C-SiC when using Si covered annealed substrates.

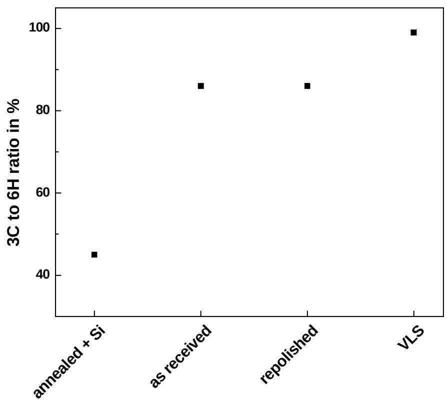

Fig. 2. Coverage of substrate by 3C-SiC in percent on differently prepared substrates.

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Evaluation of Ni and Pt Schottky barrier height in a 3C-SiC/Si vertical structure

A.E. Bazin[1,2], J.F. Michaud[1], T. Chassagne[3], M. Zielinski[3], M. Portail[4], E. Collard[2] and D. Alquier[1*]

[1] *Université François Rabelais, Tours, L.M.P, 16, Rue Pierre et Marie Curie, B.P. 7155, 37071 Tours Cedex 2, France*

[2] *STMicroelectronics, 16, Rue Pierre et Marie Curie, BP 7155, 37071 Tours Cedex 2, France*

[3] *NOVASiC, Savoie Technolac, Arche bât 4, BP 267, 73375 Le Bourget du Lac Cedex, France*

[4] *Centre de Recherche sur l'Hetero-Epitaxie et ses Applications CNRS, Rue Bernard Gregory, 06560 Valbonne, France*

[*] Corresponding author: daniel.alquier@univ-tours.fr

Due to its interesting properties and its low-cost compared to 4H-SiC, 3C-SiC is a promising material for power microelectronics. In this study, Ni and Pt Schottky barrier heights were investigated by means of a vertical structure on a polished 6 µm thick non intentionally doped 3C-SiC epitaxial layer grown on highly doped (100) Si substrate. In such a case, the substrate is taken as electrode in order to carry out a vertical conduction of the diode (see Figure 1).

To do so, a 100 nm thick Ni or Pt layer was sputtered, after a RCA cleaning step, onto the 3C-SiC surface to achieve the anode. Circular contacts with different dimensions (0.17 mm^2 to 3 mm^2) were then patterned using classical photolithography and annealed at different temperatures ranging from 500 to 900 °C. Subsequently, a Ni-Ti-Au tri-layer with thickness of respectively 100, 300 and 50 nm was sputtered directly on the silicon substrate backside. Barrier height and ideality factor were both determined by current-voltage measurements for each contact that presents a rectifying behaviour.

Figure 2 presents the current density versus forward bias J(V) plot for the 0.17 mm^2 nickel anodes as a function of the Schottky contact annealing temperature. Different behaviors are then observed. After annealing at 700 and 900 °C, the contacts seem to be ohmic while annealed at 500 and 600 °C, the Ni anodes show a rectifying behavior. For these diodes, the J(V) plot exhibits three inflexion points which are characteristic of heterogeneous diodes. This behavior could be attributed to the presence of several phases after the different annealing which could lead to several potential barriers [1][2]. The preparation of the metal/3C-SiC interface could also play a major role on this result. Unexpectedly, for a 800 °C annealing, the Ni anodes show a homogeneous Schottky characteristic. For theses diodes, the barrier height (Φ_B) and the ideality factor (η) were respectively evaluated at 0.54 eV and 1.9.

The J(V) plot for the 0.17 mm^2 platinum anodes is presented in figure 3. All the diodes exhibit rectifying behavior whatever is the temperature. However, a homogeneous behavior is obtained only after annealing at 500 and 900 °C. The best results are obtained with Pt contacts annealed at 500 °C. In this case, the barrier height and the ideality factor were respectively evaluated at 0.58 eV and 1.3 which is already an interesting result for such a structure.

For both Ni and Pt contacts, the barrier heights are much lower than the theoretical ones, respectively estimated to 1.1 and 1.85 eV. Moreover, the ideality factors are far away from the ideal value ($\eta = 1$), especially with Ni Schottky contacts. This is probably related to the presence of interface states which leads on one hand to the Fermi level pinning lowering the barrier height and on the other hand to the degradation of the ideality factor [3].

Even though low barrier height and high ideality factor are reached using this simplified process, these first results are promising for future 3C-SiC Schottky diodes. Achieving better Schottky diode characteristics can be expected with an optimized preparation of the metal/3C-SiC as well as 3C-SiC/Si interfaces.

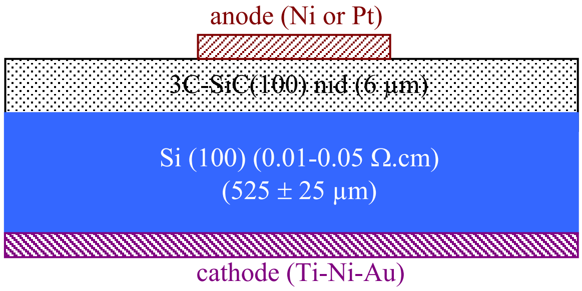

Fig. 1: Schematic view of the vertical diodes.

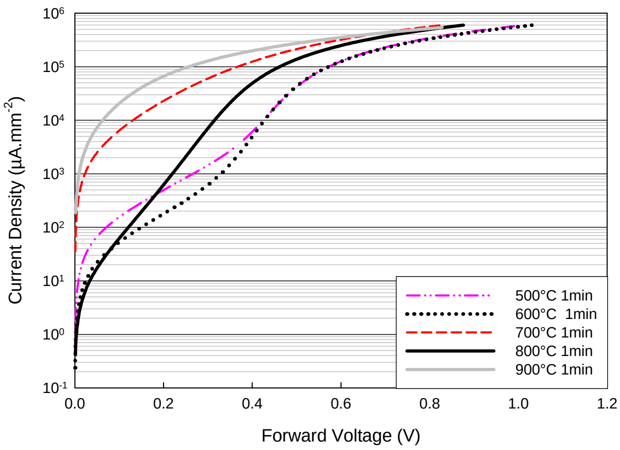

Fig. 2: J(V) forward characteristics represented for 0.17 mm^2 nickel anodes annealed between 500 °C and 900 °C.

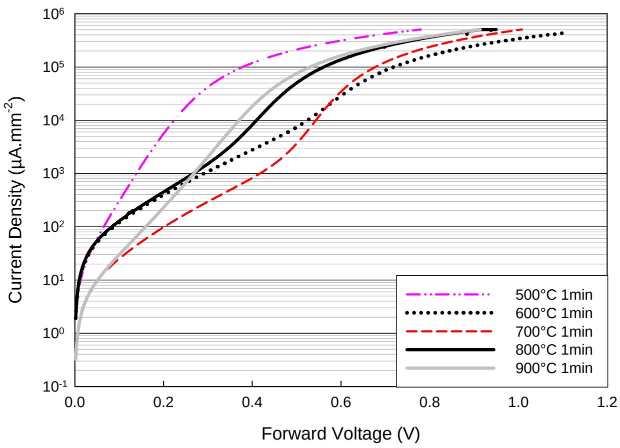

Fig. 3: J(V) forward characteristics represented for 0.17 mm^2 platinum anodes annealed between 500 °C and 900 °C.

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Effect of growth parameters on the surface morphology of 3C-SiC homoepitaxial layers grown by chemical vapor deposition

N. Jegenyes[1*], J. Lorenzzi[1], G. Zoulis[2], V. Soulière[1], J. Dazord[1], S. Juillaguet[2], G. Ferro[1]

[1]*Laboratoire des Multimateriaux et Interfaces, UMR-CNRS 5615, UCB-Lyon1, 43 Bd du 11 nov. 1918, 69622 Villeurbanne, France*

[2]*Groupe d'Etude des Semiconducteurs, CNRS and Université Montpellier 2, cc 074-GES, 34095 Montpellier cedex 5, France*

[*] Corresponding author: nikoletta.jegenyes@adm.univ-lyon1.fr

SiC is a strategic semiconductor material for electronic devices due to its unique properties that makes it applicable at high power levels and high temperature. By applying Vapour-Liquid-Solid (VLS) process, it is possible to grow high quality, twin-free 3C-SiC layers on hexagonal SiC seeds [1]. However the thickness and purity of the layers are not sufficient for the targeted electrical devices. The Chemical Vapour Deposition (CVD) method provides a solution to control the thickness of the samples by homoepitaxial growth and to grow layers of controlled n type or even p type doping level.

In this study homoepitaxial growth of 3C-SiC layers was performed using a vertical cold-wall reactor with H_2-SiH_4-C_3H_8 precursor system. The applied susceptor was made from graphite with commercial quality. The seeds were composed of a 3C-SiC layer grown by VLS method on top of 6H-SiC(0001) Si-face on-axis substrates. They all display a pronounced step-bunched morphology [2]. The samples were characterized by Nomarski optical microscopy, profilometry, micro-Raman spectroscopy and low temperature photoluminescence (LTPL).

We have studied the effect of the growth temperature and of the C/Si ratio in the gas phase on the surface morphology, the roughness and the defect density of the CVD layers. The growth temperature was varied in the range of 1450 ºC - 1650 ºC (with a constant C/Si ratio of 3) and the C/Si ratio was modified from 1 to 14.

After CVD homoepitaxial growth at temperatures below 1600 ºC and with C/Si=3 the surface structure of the 3C-SiC layers decomposed into pieces of surfaces by forming large facets (Fig. 1a). By increasing the growth temperature considerable quality enhancement can be observed: the surfaces became smooth (Fig. 1b) and the defects of the original samples were partly eliminated.

In order to confirm quantitatively the surface smoothening, the arithmetical mean roughness (Ra) of the sample surfaces was measured by applying a DEKTAK profilometer. The Ra was decreasing drastically by rising the temperature as it is shown in Figure 2a. The effect of the growth temperature on the surface defects of the VLS seeds was determined by analysing a number of Nomarski microscope images with an image processing program. The defect densities corresponding to the CVD homoepitaxial layer (ρ_d(CVD)) and the original VLS sample (ρ_d(VLS)) were obtained and compared. The fraction of these densities is shown in Figure 2b. Under 1550 ºC temperature defects were generated on the seed during the CVD growth. However at higher temperatures the ratio is less than 1, which means that the homoepitaxial layer covers the defects.

Growth temperature of 1550 ºC was applied for the C/Si ratio study. By using C/Si=1 and 10 the surface roughness, Ra decreased compared to the case of C/Si=3 (Fig. 2a), while by applying C/Si=1 Si droplets were formed on the edge of the surface. At C/Si=14 ratio the Ra roughness increased by an order of magnitude and the surface became porous. However, at C/Si=10 the ρ_d(CVD)/ ρ_d(VLS) ratio and the Ra roughness were in the same range than in the case of 1600 ºC growth temperature.

For all samples the nitrogen doping level remained below Raman detection, i.e. $<1\text{x}10^{17}$ cm^{-3} [3]. By LTPL the Al incorporation was estimated in the range of $1\text{-}10\text{x}10^{16}$ cm^{-3}. This Al contamination is caused by the used, home-made graphite susceptor and can be avoided by applying higher quality susceptor.

We can conclude that high surface quality with similar characteristics can be achieved by two different ways: (1) by increasing the growth temperature to 1600 ºC (C/Si=3) or (2) by applying lower temperature (1550 ºC) and C/Si ratio of 10.

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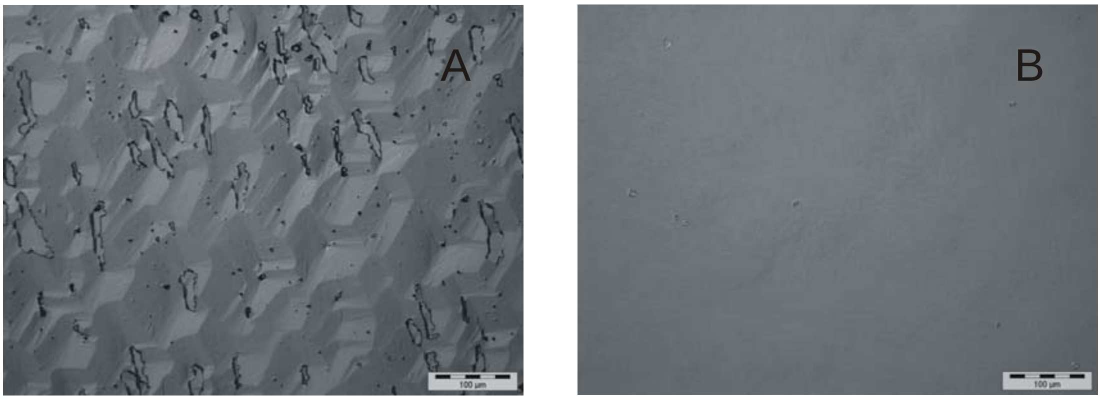

Fig. 1: The surface morphology of CVD homoepitaxial layers grown on VLS seeds by applying a) T= 1550 °C and b) T=1650 °C growth temperature with C/Si ratio of 3.

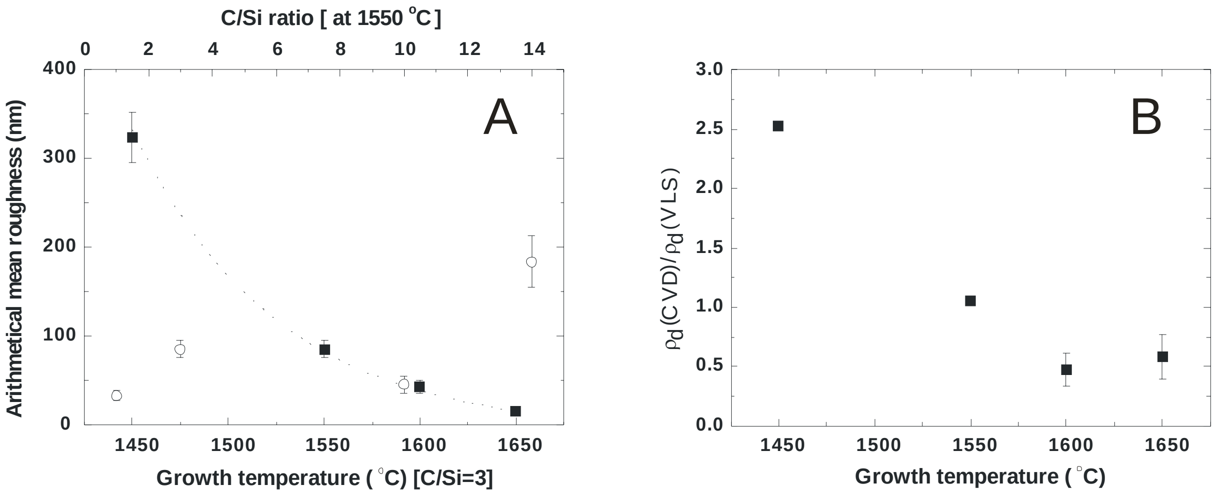

Fig. 2: Arithmetical mean roughness of the surfaces of CVD homoepitaxial layers (a) versus the applied growth temperature (■) and the C/Si ratio (○). The ρ_D(CVD)/ρ_D(VLS) defect density fraction dependence on the growth temperature is shown in figure b). The error bars correspond to statistical errors. The dashed line is guide for the eyes in figure a).

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On the structure of different long-period SiC polytypes by means of electron diffraction and high resolution transmission electron microscopy

M. Marinova[1*], E.K.Polychroniadis[1]
[1]*Department of Physics, Aristotle University of Thessaloniki, GR54124 Thessaloniki, Greece*
[*] Corresponding author: marinova@physics.auth.gr

Silicon carbide is one of the few compounds in nature that can form a variety of stable, short and long period modifications due to its one-dimensional polymorphism. The investigation of the structure and the conditions for stabilization of different long period polytypes (LPPs), as well as different polytypic transformations is very important both from fundamental and practical point of view, since the different structural symmetry changes strongly affect the electrical properties. However, despite the many years of research the driving forces for polytypism in materials are not yet very well understood and there is no unified theory explaining the appearance of that great number of polymorphic modifications. Some explanations deal with thermodynamical stability of short-period polytypes, which further serve as structural units of the LPPs [1]. On the other hand, theoretical studies [2] imply that a distortion from the ideal tetrahedron structure can favour the formation of wurzite rather than cubic structure and for this reason strain and atomic relaxation should be taken into account as important factors in the formation of a certain polytype, especially as far as heteroepitaxial growth is concerned.

The purpose of this work is to present and discuss a structural investigation of the formation of different LPPs by Electron Diffraction and Conventional and High-Resolution Transmission Electron Microscopy (HR-TEM). Analysis of diffraction patterns revealed the formation of different rhombohedral polytypes *n*R-SiC, where *n* equals 21, 27, 39, 57, 69, and 108. The exact stacking sequences of the corresponding LPPs have been determined from the HR-TEM images. The appearance of stacking fault induced inclusions of other polytypes, which lead to multi-polytipic formations, was also observed. In many cases the stabilization of these polytypes is achieved during common polytypic transformations: 1) In the 3C-6H-SiC transformation the successive formation of 21R-SiC, 39R-SiC and 57R-SiC is observed as confirmed by the selected area diffraction patterns (SADPs) shown in Fig.1. The HRTEM image in Fig. 2 reveal unambiguously the stacking sequences within the unit cells of the 21R-SiC and the 57R-SiC i.e. $(34)_3$ and $((33)_3 34)_3$, respectively. Moreover due the appearance of SFs, inclusions of 8H-SiC and 6H-SiC were seen as well in the 21R-SiC (Fig. 2(a)). 2) The formation of popytypes like 27R-SiC and 108R-SiC (Fig. 3 and Fig. 4, respectively) define in a complicated way the 6H-4H-SiC and 6H-15R-SiC polytypic transformations.

The conclusion of the above observation is that the polytype formation and the consequent mutual transformation indicate a very sensitive procedure. For this reason, even infinitesimal changes in the growth conditions or lightest strain induced by a number of different reasons can produce not only a high density of stacking faults, but also multi-polytipic sequences.

Acknowledgments:
The authors are indebted to Dr. D. Chaussende and F. Marcier from INP-CNRS Grenoble for providing the studied samples. This work has been supported by EU in the framework of the MANSiC project (Grant No. MRTN-CT-2006-035735).

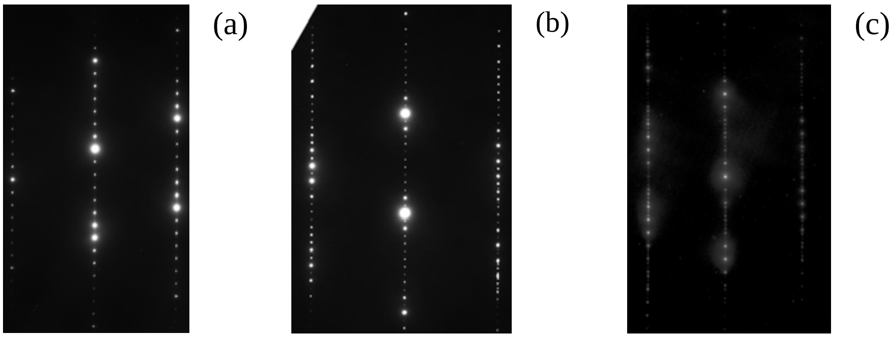

Fig. 1: SADPS confirming the 3C-6H polytypic transformation through stabilization of different rhombohedral LPPs: (a) 21R-SiC; (b) 39R-SiC and (c) 57R-SiC.

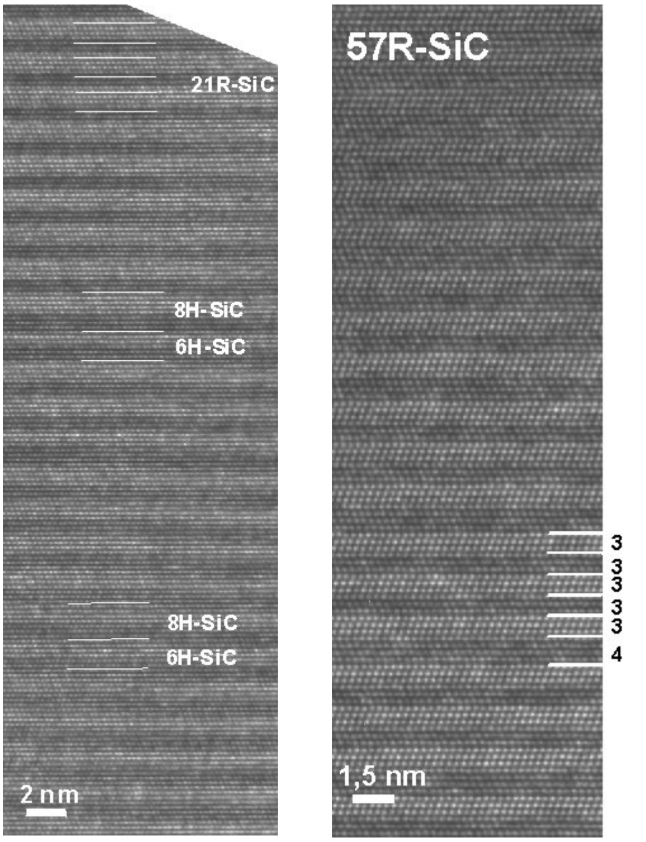

Fig. 2: HRTEM micrographs from (a) 21R-SiC showing the formation of SF induced lamellae of different polytypes; and (b) 57R-SiC.

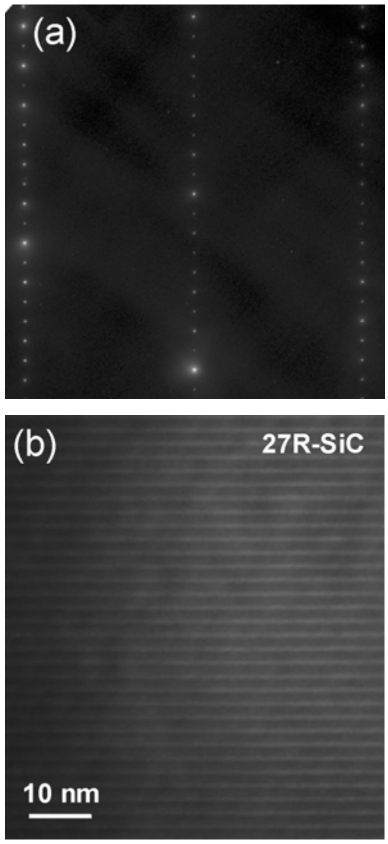

Fig. 3: (a) SADP revealing the formation of 27R-SiC (b) conventional XTEM image.

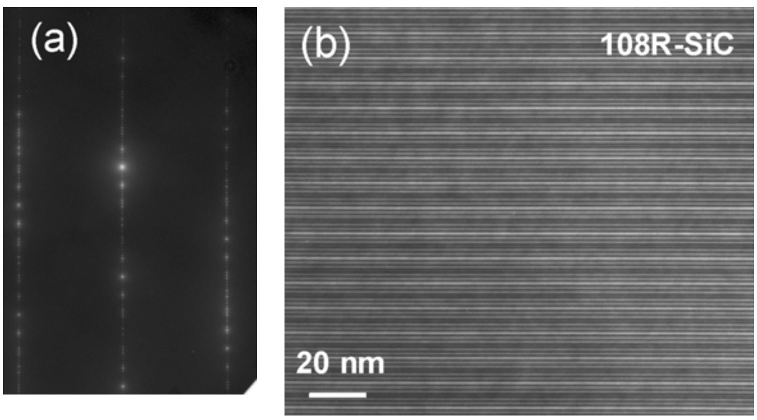

Fig. 4: (a) SADP revealing the formation of 108R-SiC (b) conventional XTEM image.

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Observation of 3C zigzag faults in low-doped 4H-SiC epitaxial layers

T. Robert[1], M. Marinova[2], S. Juillaguet[1], A. Henry[3], E.K. Polychroniadis[2], J. Camassel [1,*]
[1] *Groupe d'Etude des Semiconducteurs, Université Montpellier 2 and CNRS, cc 074-GES, 34095 Montpellier Cedex 5, France*
[2] *Department of Physics, Aristotle University of Thessaloniki, GR54124 Thessaloniki, Greece*
[3] *IFM departement, Institute of Technology, Linköping University*
[*] Corresponding author: camassel@univ-montp2.fr

Low-doped epitaxial layers are mandatory to develop high power SiC devices. Unfortunately in such layers stacking faults (SFs) often appear, which are well-known defects in 4H silicon carbide (4H-SiC). They manifest as a stable lamella of a different polytype, with a finite thickness and a finite lateral extension in the basal plane. In the case of 4H-SiC, most of the in-grown SFs identified up to now come from a combinations of single Shockley staking faults (SSF) and have, either, the 3C [1,2] or 8H [3,4] polytype structure. In both cases, since the faulted polytype has a smaller bang gap energy than the one of the host material, they behave like a thin type-II quantum well (QW) embedded in the 4H-SiC matrix. This point is now well established [2, 5, 6] but, in this work, we show that 3C-like zigzag faults can also exist in 4H-SiC.

We focus on a 4H-SiC epitaxial layer grown in a commercial hot-wall reactor. The substrate was a highly doped 4H-SiC wafer (Si face, 8° off) from SIXON, with residual doping ~ 10^{19}cm^{-3}. The layer had a thickness of about 30 µm and was intentionally nitrogen doped to ~ 10^{15}cm^{-3}. A first result is that, using Low Temperature Photoluminescence (LPTL) spectroscopy, we could not resolve the usual near band excitonic (NBE) features specific of low doped 4H-SiC. Instead we obtained optical SFs signatures varying rapidly from spot position to spot position, which indicated in-grown SFs. A typical LTPL spectrum is shown in Fig 1. From the energy of the momentum-conservative TA, LA, TO and LO phonon replicas, we deduce for the two different features a fundamental recombination energy (excitonic energy gap) $E_{g(X)}(1)$ = 2.98 and 2.79 eV. This suggests (see Ref. [6]) two and three bilayers (BLs) thick lamellae of 3C-SiC, respectively, embedded in the 4H-SiC matrix.

To get confirmation of this assignment, and clarify the origin of the dispersion in SFs signatures, we performed high-resolution TEM measurements in a neighbouring area. Results are shown in Fig.2. Clearly, on the cross-sectional image one identifies three different defects (faulted stacking sequences) which have been noticed SF(1), SF(3) and SF(4). All have the same general aspect, but do not confirm the 3C or 8H picture. Rather, they are made of an even or odd number of half-unit cells of 6H-SiC which define specific 3C zigzag faults. In the Hägg notation, each defect corresponds to a specific (twisted) arrangement of one or more successive (+++) and (---) 3C lamellae.

When the fault is only a half unit cell of 6H-SiC like SF(1), it appears like a single (three BLs thick) lamella of 3C and, in this case, the formation mechanism is simple. It can be easily described as a single Schokley staking fault SSF(3,1) or a Franck fault in between two 4H-SiC planes. When the chain extension increases, like the one in SF(3) and SF(4), the description in terms of specific combinations of elementary SSFs becomes increasingly difficult. For instance, one would need two elementary SSFs separated by 5 BLs of 4H-SiC to build a single 6H unit cell (or SF(2), not shown in Fig.2) while concerning SF(4) one would need 4 Franck faults or 6 elementary SSFs in arrangement (++--++|+-|-|-|+|++|---++--). Concerning SF(3) we could not find any description in term of elementary SSF and, to the best of our knowledge, only Frank faults should be used.

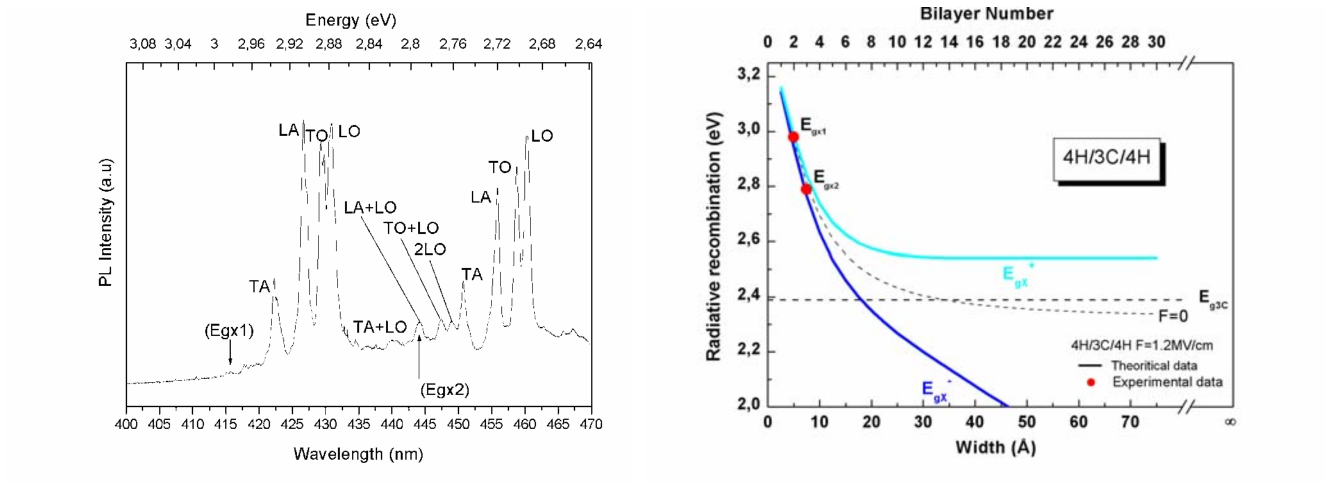

Fig. 1: Example of LPTL spectra collected at 5K, respectively on the 4H-SiC epitaxial layer considered in this work. From the phonon-assisted TA, LA, TO, LO replicas, two excitonic energy gaps indicative of 2 and 3 BLs thick 3C lamellae are deduced.

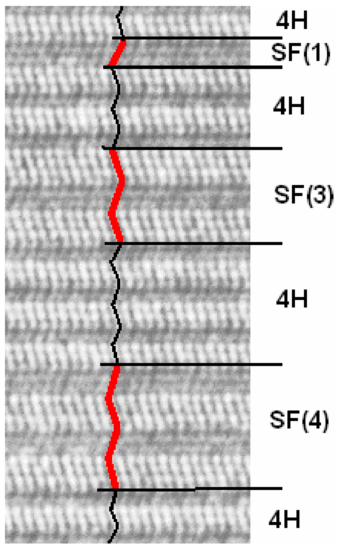

Fig. 2: Cross-sectionnal high resolution TEM image of various 3C-like zigzag faults in 4H-SiC. SF(1), SF(3) and SF(4) mean, respectively, 1, 3 and 4 zigzagged sequences of 3 bilayers of 3C.

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"In situ" Low Temperature Photoluminescence in ion irradiated 4H-SiC

G. Litrico[1,*], M. Zimbone[1], L. Calcagno[1], P. Musumeci[1], G. A. Baratta[2] and G. Foti[1]
[1]*Department of Physics and Astronomy, University of Catania, Italy*
[2]*INAF- Astrophysical Observatory, University of Catania, Italy*
[*] Corresponding author : grazia.litrico@ct.infn.it

Low Temperature (40 K) Photoluminescence was used to follow the defects formation in 4H-SiC epitaxial layers induced by irradiation with 200 keV H+ beam in the fluence range $6.5 \times 10^{11} - 1.8 \times 10^{13}$ ions/cm^2. Ion irradiation was performed at low temperature in small fluence steps (3.5×10^{11} ions/cm^2). After each irradiation step the LTPL spectrum was acquired.
The defects produced by ion beam irradiation induce the formation of some sharp lines called "alphabet lines" in the photoluminescence spectra in the 425-443 nm range, due to the recombination of excitons at structural defects.
The un-irradiated sample was characterized by LTPL on a broad wavelength range (380-600 nm) and its luminescence spectrum shows free exciton lines (FE) and N-bound exciton lines in the wavelength range 382-392 nm, thus indicating a good crystal quality.
The luminescence spectra in the range 425-443 nm of the un-irradiated sample and of different fluence irradiated samples are reported in Fig. 1. The un-irradiated sample spectrum does not show any peak in this wavelength range, indicating that the spectral peaks detected in the irradiated samples are related to ion induced defects, indeed the peak intensities change as a function of the ion fluence. In particular in the spectrum of the sample irradiated with a fluence of 25×10^{11} ions/cm^2 we can clearly distinguish seven luminescent peaks that are the well known alphabet lines *a-g*.
Egilsson et al. [1] suggest that these alphabetic lines are due to bound- to-bound-state transitions and do not involve free carriers and they propose bound exciton recombination at isoelectronic defects centres with a complex structure related to a silicon vacancy. Eberlein et al. [2] instead argue that these lines are due to the recombination of a delocalized electron with a localized hole bound to a Si antisite defect in proximity of a C antisite.
The trend of LTPL lines intensity as function of proton fluence, allows distinguish two different groups of peaks, namely the P_1 group (*e, f, g lines*) and the P_2 group (*a, b, c, d lines*).
The normalized yield of the P_1 group lines (reported in Fig.2) shows an increase with ion fluence, until a maximum value at a fluence of 2.0×10^{12} ions/cm^2 is reached and then an abrupt decrease at higher fluence. At fluences $\geq 1.5 \times 10^{13}$ ions/cm^2 the yield of these lines is 20% of its maximum value. In the insert is show the detailed behaviour of these lines in the low fluence region ($<3.0\times10^{12}$ ions/cm^2). The data show an almost linear increase of the yield with fluence indicating that the related defects are associated to the primary ion beam defects (vacancies or interstitials).
An almost similar behaviour is shown by the P_2 lines (*a-b-c-d*) (Fig.3), whose intensity increases at low fluences, it reaches the maximum at a fluence of 2.5×10^{12} ions/cm^2, but at higher fluence it decreases to 50% of the maximum value. The detailed analysis in the low fluence range shown in the insert of Fig.3 indicates that the yield of these lines is almost negligible at fluences lower than 6.5×10^{11} ions/cm^2 and from this value (threshold fluence) it increases.
This threshold for the P_2 lines formation indicates that the defects associated to these lines could be related to complex defects, because they are formed only when a critical density of primary defects (interstitials or vacancies) is produced by the ion beam. The value of this critical defect density is 1.5×10^{16} vacancies/cm^3, corresponding to a mean defect distance of 40 nm: when the mean distance between primary defects is less than 40 nm, their interaction rises to the nucleation of complex defects.

The decrease of P_1 and P_2 normalized yields at high fluence values should be related to a decrease of free carriers and/or to a modification of the related defects. The decrease of carriers concentration should reduce the intensity of both P_1 and P_2 lines simultaneously, whereas experimental data show a decreasing rate higher for the P_1 lines than for the P_2 lines. This behaviour indicates that probably the defects associated to the P1 lines are partially recombined at high fluence. This recombination is lower or negligible for the defects associated to the P_2 lines.

The threshold at low fluence and the low recombination rate at high fluence observed for the P_2 luminescence lines are both consistent with the hypothesis that these lines are associated to complex defects.

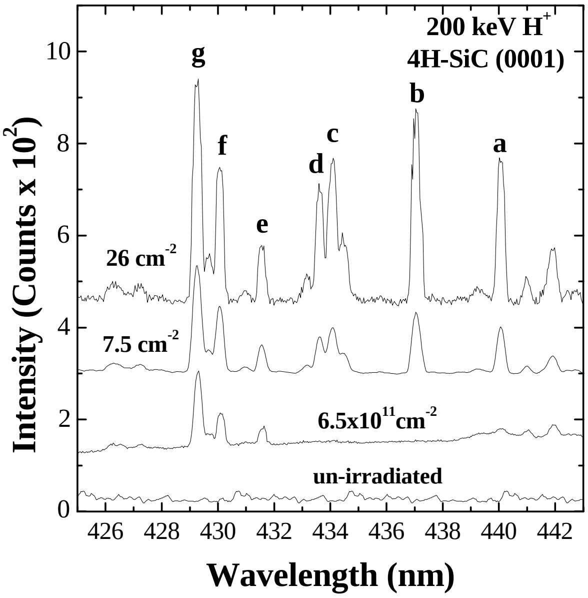

Fig.1: LTPL spectra (40 K) of the un-irradiated 4H-SiC sample and of different fluence irradiated

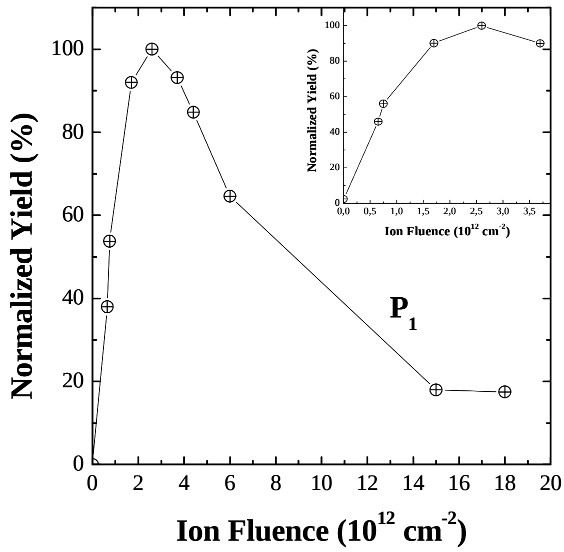

Fig 2: Normalised yield of P_1 line group as a function of proton fluence. In the insert the low fluence range behaviour is shown.

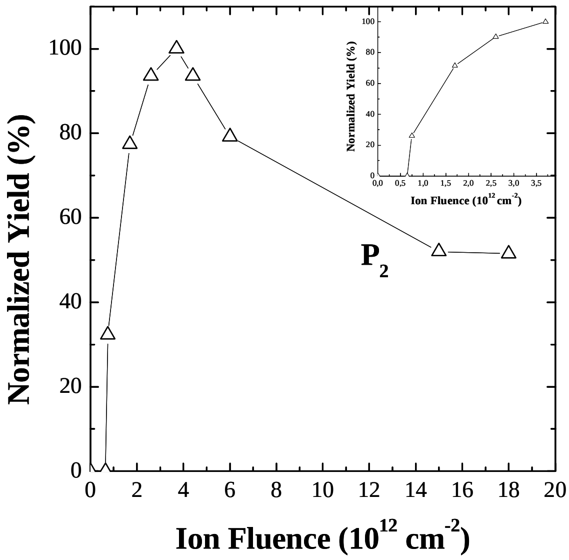

Fig 3: Normalised yield of P_2 line group as a function of proton fluence. In the insert the low fluence range behaviour is shown.

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Electrical and optical properties of *p*-type ZnO films grown on sapphire

J. W. Sun[1, 2*], Y. M. Lu[1], Y. C. Liu[1], D. Z. Shen[1]
[1]*Key Laboratory of Excited State Processes,*
Changchun Institute of Optics, Fine Mechanics and Physics,
Chinese Academy of Sciences, 130033 Changchun, P. R. China
[2]*Present Address: Groupe d'Etudes des Semiconducteurs, Université Montpellier 2 and*
CNRS, cc 074-GES, 34095 Montpellier Cedex 5, France
[*] Corresponding author: jianwu.sun@ges.univ-montp2.fr

In the recent years, ZnO has attracted much research interest as a strong candidate for light emitting devices. Based on a large breakdown voltage and high saturation velocity, ZnO is also a suitable candidate for RF electronic device applications [1, 2]. The availability of high-quality *p*-type ZnO is then necessary to develop photonic and electronic devices.

In this work, nitrogen-doped *p*-type ZnO films were grown on c-plane sapphire by plasma-assisted molecular beam epitaxy, using radical NO as oxygen and nitrogen sources. The research effort was concentrated on the acceptor-related recombination mechanisms and the hole transport properties in nitrogen-doped *p*-type ZnO films.

Table I presents three *p*-type ZnO samples with different electrical properties at room temperature (RT). X-ray diffraction results shows the *p*-type ZnO films have a high c-axis orientation with a wurtzite structure. X-ray photoelectron spectroscopy measurements clearly demonstrate that nitrogen is incorporated in oxygen site, being the desired acceptor, in N-doped ZnO films.

Figure 1 compares 80 K photoluminescence (PL) spectra of the undoped and *p*-type ZnO films (sample A). The spectrum of the undoped ZnO is typically dominated by a free exciton (FE) peak at 3.377 eV and a neutral donor-bound exciton (D^0X) at 3.363 eV, with two weaker broad lines centered at 3.313 and 3.240 eV which are assigned to the longitudinal optical (LO) phonons, respectively. While the *p*-type sample A has a strong line at 3.263 eV, with three gradually weaker broad lines centered at 3.191, 3.119, and 3.047 eV, respectively. Since the emission at 3.263 eV exhibits an obvious blueshift with increasing excitation intensity, we attribute it to a DAP transition. The three shoulders at lower-energy side of DAP are assigned to DAP-LO, DAP-2LO, and DAP-3LO, respectively. The peak at 3.322 eV is assigned to the free electron to acceptor (FA) recombination by studying the temperature evolution of DAP and FA peaks. For samples B and C, the DAP peaks significantly dominate the spectrum and slightly shift to 3.258 eV. And the FA peaks slightly shift to 3.317 eV. In addition, the acceptor binding energy is estimated to be about 120 ~145 meV by PL results.

The transport properties of *p*-type ZnO films were investigated by temperature-dependent Hall-effect measurement. As shown in figure 2, the experimental hole mobility was found to be considerably lower than the calculated mobility including ionized impurity scattering (μ_i), acoustic-mode deformation potential scattering (μ_{as}), acoustic-mode piezoelectric potential scattering (μ_{pz}), and polar optical phonon scattering (μ_{pop}). It was found that *p*-type ZnO on c-Al_2O_3 consisted of two kinds of 30º-rotated domains surrounded by grain boundaries by Atomic force microscopy and XRD Φ-scan of (103) reflection measurements. Heleskivi and Salo suggested a model to consider the Hall coefficient in an inhomogeneous material included the grains and the grain boundaries [3]. We used this model to evaluate the effect of this inhomogeneous microstructure on the mobility in *p*-type ZnO (The curves of $\mu_{m,m1,m2}$ were the calculated values by Heleskivi and Salo's model for different parameters.). It was found that the calculated mobility agreed with the experimental data. This indicates that the low mobility in *p*-type ZnO is mainly determined by the inhomogeneous microstructure including columnar grain size and grain boundaries.

Table I : RT electrical properties of N-doped *p*-type ZnO films

Sample	Carrier concentration (cm^{-3})	Mobility (cm^2/Vs)	Carrier type
A	6.88×10^{16}	0.96	*p*
B	4.35×10^{17}	0.22	*p*
C	1.22×10^{18}	0.45	*p*

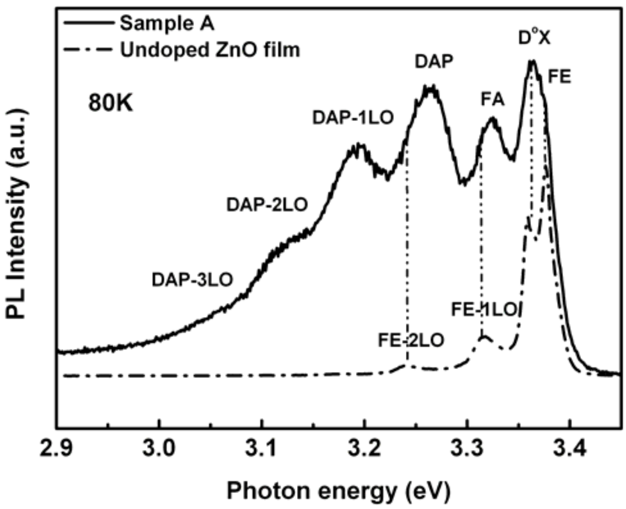

Fig. 1: PL spectra of undoped ZnO and N-doped *p*-type ZnO (sample A) at 80 K

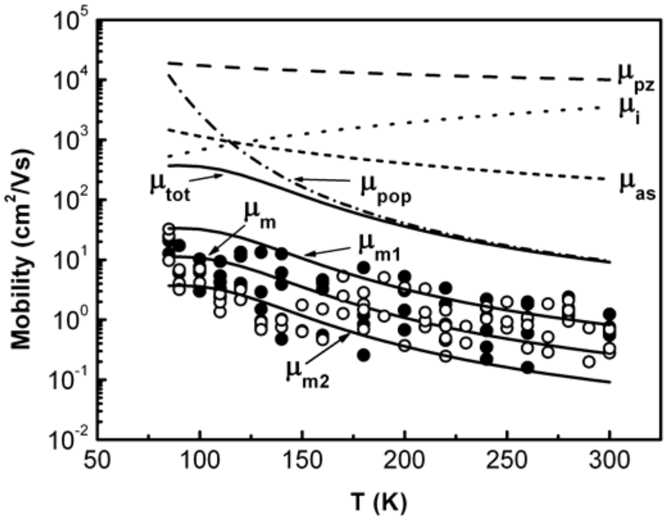

Fig. 2: Experimental and calculation hole mobility as a function of temperature for the *p*-type ZnO films

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Two-dimensional electron gas isolation in AlGaN/GaN devices

F. Roccaforte[1*], F. Iucolano[1], F. Giannazzo[1], S. Di Franco[1], G. Abagnale[2], V. Puglisi[2], V. Raineri[1]
[1] *CNR-IMM, Strada VIII, n.5, Zona Industriale, 95121 Catania – Italy*
[2] *ST Microelectronics, Stradale Primosole 50, 95121 Catania – Italy*
[*] Corresponding author: fabrizio.roccaforte@imm.cnr.it

AlGaN/GaN heterostructures are superior materials for high-frequency and high-power devices. In fact, the spontaneous and piezoelectric polarization charges generate a two dimensional electron gas (2DEG) at the AlGaN/GaN interfaces, with high sheet carrier densities and carrier mobility, suitable for fabricating high electron mobility transistors (HEMTs) working up to several tens of GHz. Typical applications of these devices are in base stations for mobile phones, high-power radar systems, etc..

The knowledge of the near-surface modifications performed to locally tailor the 2DEG properties is one of the fundamental issues in GaN technology, because of the applications for inter-device isolation, normally-off HEMTs operation, etc. Inter-device isolation is typically obtained by means of mesa etch, nitrogen ion-implantation or local thermal oxidation. However, the integration of these processes in the complete device fabrication can affect the 2DEG properties and, hence, the device performances.

In this work, the physical aspects related to different 2DEG isolation processes are discussed.

AlGaN/GaN heterostructures grown on sapphire were used. The structure was composed by a 3 μm thick insulating GaN layer, followed by a 10 nm thick n-type Si-doped GaN carrier supplier layer (with a carrier concentration $N_D \sim 10^{18}$ cm^{-3}), and a 50 nm thick n-type $Al_{0.28}GaN$ barrier layer on the top (with $N_D \sim 5\times10^{17}$cm^{-3}).

For the electrical characterization of the isolation process, appropriate test patterns were fabricated (see Fig. 1). Isolation by nitrogen ion-implantation was obtained by multi-energy implants, with energy in the range 20-80 keV, and doses in the range of $1\text{-}5\times10^{13}$cm^{-2}. Selective local oxidation of the AlGaN surface region was performed at 900°C in O_2, on lithographically patterned samples using a thick SiO_2 mask [1]. Ohmic contacts were formed using an annealed Ti/Al/Ni/Au stack [2,3]. Test HEMTs devices and lateral MOS structures were also fabricated to determine the 2DEG electrical properties. The electrical characterization consisted of current-voltage (I-V) and capacitance-voltage (C-V) measurements. Scanning capacitance microscopy (SCM) on beveled samples [4], both in oxidized and in non-oxidized regions, allowed to get further insights on the carrier profiles.

As can be seen in Fig. 2, when using nitrogen-implantation for isolation, a decrease of the sheet resistance of implanted regions occurs when the sample is subsequently subjected to the thermal budgets typically used for optimal Ohmic contacts [2,5]. Alternatively, selective thermal oxidation can be an efficient stable 2DEG isolation process [6], comparable to mesa etch, but high-temperature annealing is required (900°C). Fig. 3 shows the I-V curves of test-patterns for 2DEG isolation by selective thermal oxidation. It is interesting to point out that 2DEG isolation is achieved even if the thickness of the formed thermal oxide layer does not reach the AlGaN/GaN heterointerface, as can be seen from the TEM image of the sample oxidized at 900°C for 12 h (Fig. 4) [1]. The structural analysis indicated the formation of both α-Al_2O_3 and β-Ga_2O_3 phases. I-V and C-V measurements performed on HEMTs, fabricated both on the as-grown AlGaN/GaN material, and on the samples that were undertaken to an oxidizing annealing at 900°C (in the presence of the SiO_2 capping layer), showed a reduction of the sheet carrier density n_s (from 9.2×10^{12}cm^{-2} to 4.4×10^{12}cm^{-2}) and a shift of the threshold voltage of 5.3 V towards less negative values. Scanning capacitance microscopy analysis allowed to ascribe the electrical results to a dopant deactivation, that can be associated to the compositional instability of the material during high temperature annealing [2].

Finally, tailoring of the 2DEG properties could be demonstrated by an inductively plasma etch (ICP) process in CHF_3/Ar, that can be alternative to the conventional reactive ion etching (RIE) process in CF_4 [5]. In particular, with increasing power of the RF-source, the plasma-induced damage increased and, hence, a reduction of n_s occurred. However, C-V analysis showed that post-annealing treatments at temperatures between 400 and 500°C, i.e. compatible with HEMTs devices fabrication, are able to remove the plasma-induced damage and almost completely recover the electrical properties of the 2DEG, resulting in a shift of the threshold voltage towards the normally-off operation mode.

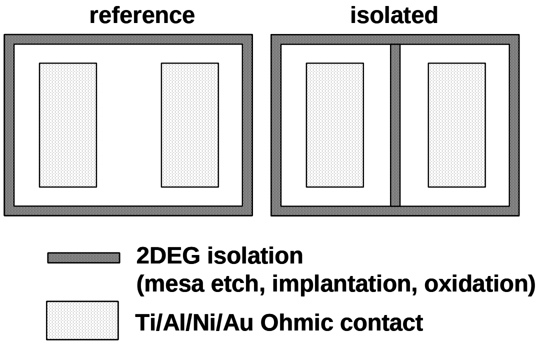

Fig. 1: Schematic of the structures used for testing the 2DEG isolation

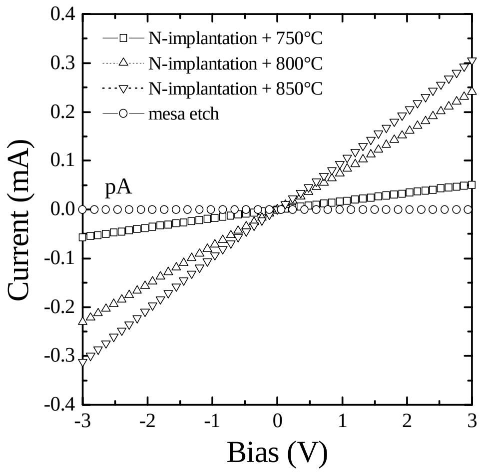

Fig. 2: I-V curves measured in structures isolated mesa etch or nitrogen implantation. Thermal annealing lead to a decrease of the sheet resistance of the N-implanted region

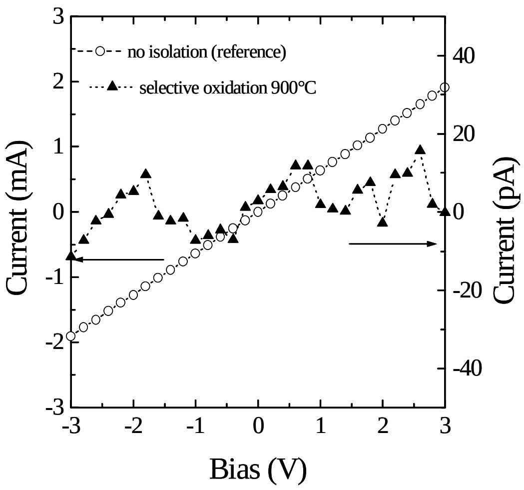

Fig. 3: I-V curves measured in structures isolated by selective oxidation at 900°C. The I-V curve of the reference sample (no isolation) is also reported

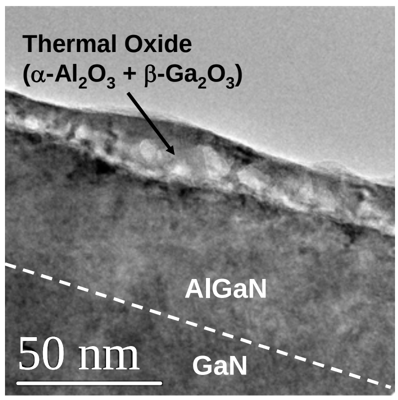

Fig. 4: Cross section TEM image of the AlGaN/GaN sample after annealing in O_2 at 900°C

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Electron mobility in GaN solving the Boltzmann equation

C. Miccoli[1,2,*], A. Majorana[3]
[1]*Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, I-95123 Catania, Italy*
[2]*ST Microelectronics, Stradale Primosole 50, 95121 Catania, Italy*
[3]*Dipartimento di Matematica e Informatica, Università di Catania, Via S. Sofia 64, I-95123 Catania, Italy*
[*] Corresponding author: cristina.miccoli@st.com

Recently, III-nitride compounds have received vast attentions and considerations, because gallium nitride (GaN), aluminium nitride (AlN) and indium nitride (InN) have a wide band-gap and they have a very large range of applications, from optoelectronics (LED and LASER) to power devices (HEMT, Schottky diode) [1]. GaN seems to be the best candidate to overcome silicon limitations, really it has a direct band-gap, a moderately high mobility (~1500 cm^2/V s) and high critical electric field (~3.4E6 V/cm)[2-5]. These physical parameters are useful for high-power/high-frequency devices.

Nevertheless many aspects remain to be investigated and GaN is not fully characterized by experiments. Some parameters of interest can be evaluated with numerical simulations, like energy band levels, electric fields, velocities, charges, etc., being impossible to extract this kind of parameters from a real device even using experimental analysis. Therefore, it is necessary to study and realize predictive models, because physics-based simulators and modelling tools are of great importance for GaN based transistor design and also fundamental to understand the physical phenomena that appear in this kind of devices [6]. In this contribution, the transport properties of GaN bulk will be discussed starting from Boltzmann equation.

The band structure of the material under study is approximate with an analytical formulation using nonparabolic spherical valleys [7]. In order to calculate the electron drift velocity in reference to electric field in GaN-bulk, consideration of conduction band satellite valleys is necessary. For wurtzite-phase GaN, we consider a three-valley system: the minimum of the conduction band Γ_1, a higher energy band Γ_2, and six L-M equivalent bands. The band parameters can be found in Refs. [8-11]. The dispersion relation in each valley is given by the Kane model, because it is simple but also suitable to describe the high field regime.

For the electron gas in GaN we take in account both Boltzmann equation and Poisson equation, in order to study the linear transport in each valley and the electrostatic interaction through the electric potential V and its field E. Hence, we have three Boltzmann equations in correspondence of the three valleys.

The collision operator of each Boltzmann equation contains the scattering linear operator S_A (A = Γ_1, Γ_2, L-M) which take into account the interactions of the electrons with the crystal vibrations. The total amount of the scattering process is summarized in the collision operator Q_A. In particular, we included in the simulation the following scattering mechanisms: acoustic phonon, polar optical phonon, deformation potential, nonpolar optical phonon (intervalley scattering) and ionized impurity scattering.

The numerical method is inspired by the scheme in [13] referred to Silicon device, here we adapt and set all the parameters for GaN-bulk semiconductor. Important numerical difficulties are the conservation of charges due to the involved intervalley scatterings and the collision operator, in which all integrals concerning the singular kernels can be computed explicitly. As the scheme reported in [13], the deterministic numerical results show a high order of accuracy and the distribution function, with all its moments, is computed correctly. Moreover, it is possible to study the transient solution of the system.

In Figure 1 and 2 the average energy and the drift velocity are reported. The values are in agreement with [9]. So, the numerical scheme and the physical model are well defined and validate. Surely, simulation results can play a key role in order to understand the trend of physical process in the GaN-bulk. This is also a starting point for the enlargement of that method to the other Nitride compound (AlN, AlGaN, etc.). Finally, the numerical model is suitable to modify and/or add new contributions of the scattering mechanisms that are present in the material and they can help us to study and analyze GaN-based device.

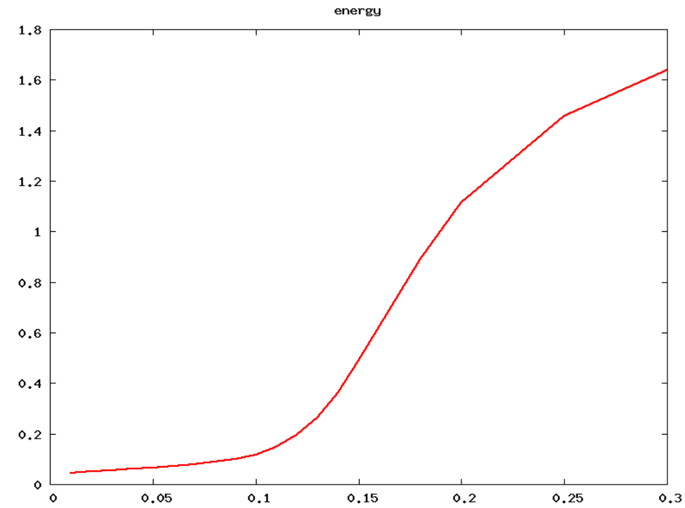

Fig. 1: Calculated average energy (eV) as function of the applied electric field (MV/cm) in bulk wurtzite GaN.

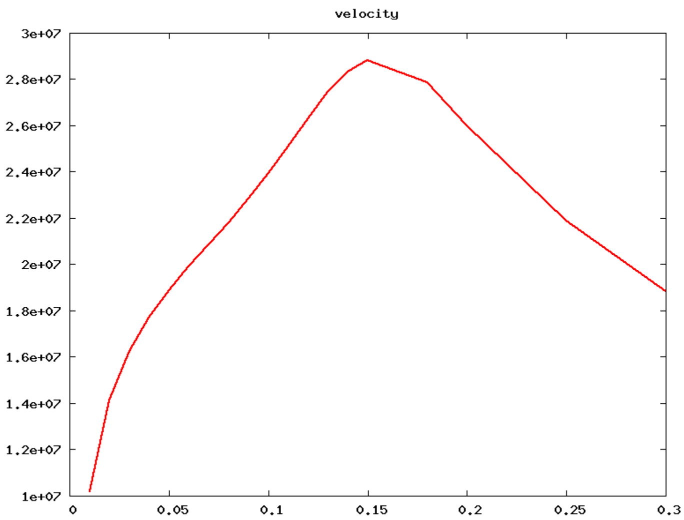

Fig. 2: Calculated electron velocity (cm/s) as function of the applied electric field (MV/cm) in bulk wurtzite GaN at 300 K.

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Defects and electrical activation of Al ion-implanted 4H-SiC for power MOSFETs

M.H. Weng[1*], F. Roccaforte[1], F. Giannazzo[1], R. Lo Nigro[1], C. Bongiorno[1], S. Di Franco[1], E. Zanetti[2], A. Ruggiero[2], M. Saggio[2], V. Raineri[1]
[1] *CNR-IMM, Strada VIII n. 5, Zona Industriale, 95121, Catania, Italy*
[2] *ST Microelectronics, Stradale Primosole 50, 95121, Catania, Italy*
[*] Corresponding author: minghung.weng@imm.cnr.it

The need of low resistive contacts to avoid internal power loss is an obvious mission in the coercive voltage devices. For silicon carbide (SiC) power MOSFETs, ion implantation has been widely accepted as the most suitable process to achieve selective doping where low resistive contacts should be formed. However, irradiation to implant and high temperatures post-annealing to active dopants normally lead to destructive lattice damage in the material. These defects can significantly influence the electrical properties of the implanted layer and eventually to Ohmic contacts, which result in the degradation of device performance. Therefore, comprehensive study is needed to understand the radiation damage, with the electrical activation of the implanted species and Ohmic contacts behavior, in ion-implanted SiC to achieve a functional power device.

N-type substrate with an epitaxial layer thickness of 0.5 μm and a net donor concentration of 1×10^{18} cm^{-2} were used to study the electro-structural properties of p-type ion-implanted 4H-SiC. Aluminum (Al) ion at energies between 30 and 80 keV and fluences in the range 0.3-1×10^{15} cm^{-2} were implanted, followed by post-annealing processes at temperatures of 1650°C for 30 minutes, in order to achieve a p-type enrichment (p+) region near the surface. Ohmic contacts were formed by deposition of Ti/Al bilayers, and annealed in the temperature range of 900-1000°C. In this region, Ohmic contacts formed upon annealing at 1000°C, the electrical properties were determined by Transmission Line Model (TLM), Hall measurement, and 4-point probing structures. The surface roughness was calculated as the root mean square (RMS) and doping profiles were determined by Atomic Force Microscopy (AFM) and Scanning Capacitance Microscopy (SCM), respectively.

The characterizations of the implanted sample were divided into topographical and electrical measurements. After implantation and post-annealing on unprotected samples, a high surface roughness was observed, i.e. RMS=9.14 nm for a 20 μm × 20 μm scan as shown in Fig. 1. A section analysis shows "ripples" created on the surface by step bunching. The averaged distance of 0.82±0.5 μm was observed between ripple peaks. Transmission electron microscopy (TEM) analysis was used to conduct structural cross-section study. Fig. 2 shows an image of p-type enrichment and body implantation profiles. In addition, the surface of cross-section also shows a wave-lined topography (estimated average peak to peak distance of 0.8 μm) which corresponds to the ripples observation of step bunching earlier by AFM. Moreover, precipitates were both observed in the p-type enrichment close to surface and in the middle of body implanted areas. These aspects have been further studied for activation/compensation of the implantation by SCM. Fig. 3 shows the normalized SCM signals with illustration of precipitates. It is observed low activation in the doping profiles, especially in the near surface and middle range of body areas. The results suggest low activation near the surface is due to the facts that inactive dopants and precipitates are presented in this region. In our previous study [1], an inactive Al specie or extra impurity could result in compensation of desired activation of implanted regions. As result, the value of the sheet resistance (R_{SH}) extracted by TLM was in the order of 28.5 kΩ/square. The high value of R_{SH} is not only due to the low activation of the Al implanted specie, but also to the ion-induced damage in the material (both bulk defects and surface defects), as a low value of hole mobility of 20.7 cm^2/V-s was determined by Hall measurement.

In conclusion, the structural defects of step bunching were first studied by AFM. The surface ripples were correlated by plenary (AFM) and cross-section (TEM) studies. TEM analysis also revealed sub-surface defects, where precipitates were found as inactive impurities in both near surface and body implanted profiles. Electrical activations and properties were obtained in low activated areas.

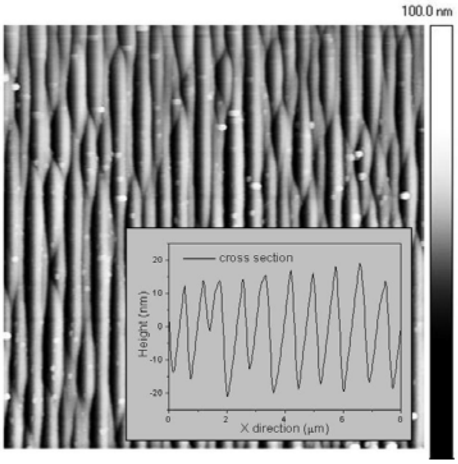

Fig. 1: AFM image of step bunching structures and the corresponding height across the ripples.

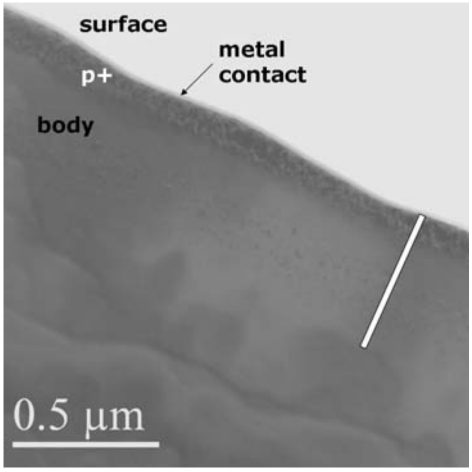

Fig. 2: TEM micrograph of Ti/Al bilayers deposited on Al ion-implanted 4H-SiC.

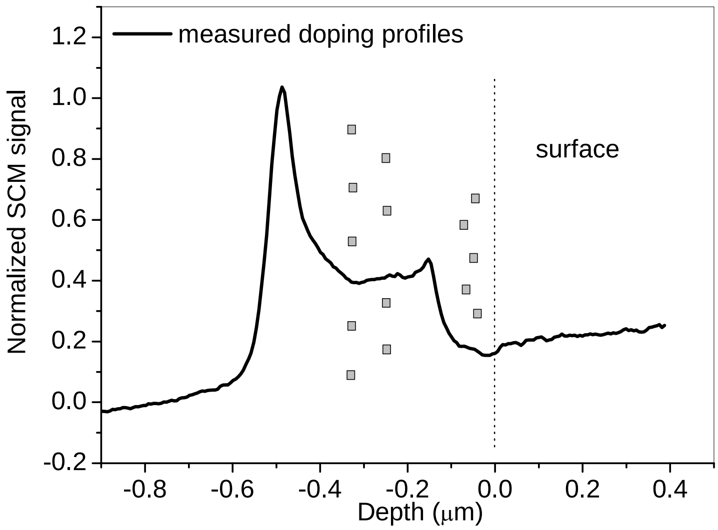

Fig. 3: Measured SCM signals, filled squares illustrate the precipitates which were found in the TEM image.

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Nanoscale electrical characterization of wide-bandgap semiconductors materials and devices

F. Giannazzo *, F. Roccaforte, F. Iucolano, Ming-Hung Weng, S. Di Franco, V. Raineri
CNR-IMM, Strada VIII n.5, Zona Industriale, 95121 Catania, Italy
* Corresponding author: filippo.giannazzo@imm.cnr.it

One of the crucial requirements to assess a mature technology on wide-bandgap semiconductors (SiC, GaN) is the high resolution and quantitative determination of the transport properties of the material (carrier concentration, mobility) and of the interfaces with dielectrics and metal layers. Different applications of scanning probe microscopy, allowing to access to all of these properties on nanoscale, are illustrated in this paper.

Ion implantation is the method of choice for selective area doping of SiC and GaN and for device isolation. High thermal budgets are typically required to activate dopants and to anneal those defects acting as compensating and/or scattering centres. Hence, methods allowing to determine the depth profiles of carrier concentration and mobility are highly desirable. Quantitative scanning capacitance microscopy (SCM), yielding the net doping concentration profile in a semiconductor, and scanning spreading resistance microscopy (SSRM), yielding the resistivity profile, were jointly applied to determine the profiles of active dopants, of compensating defects and of the drift mobility, for different implant and annealing conditions [1]. In particular, we systematically studied the effect of the annealing temperature on the evolution of the acceptor (N_A) and compensating centers (N_{comp}) concentration in a 4H-SiC layer implanted with multiple energy and medium dose (1×10^{13} cm^{-2}) Al ions. According to TRIM simulations, this Al dopant profile could produce a medium concentration (~10^{18} cm^{-3}) uniformly doped p-type layer, if all Al atoms occupy substitutional positions. The measured profiles of N_A, N_{comp} and of the net dopant concentration (N_A-N_{comp}) are reported for two annealing temperatures (1500 and 1650 °C) in Fig.1(a) and (b), respectively. The peculiar shape of the net doping profiles can be clearly explained in terms of the evolution of N_A and N_{comp} with the annealing temperature. In fact, at 1500 °C the higher values of N_{comp} are responsible of the electrically inactive surface region (~100 nm thick) in the N_A-N_{comp} profile. After annealing at 1650 °C, N_{comp} becomes a smaller fraction of N_A, and the net doping profile is almost coincident with the N_A profile. By calculating the area under the N_A and N_{comp} profiles in the implanted region, the doses of the acceptors (D_A) and compensating centres (D_{comp}) were obtained. Furthermore, the evaluated drift mobility profiles for the two annealing temperatures are reported in Fig.1(c) and (d).

The electrical behaviour of the metal-semiconductor devices depends on the nanoscale lateral homogeneity of the Schottky barrier (SB). Hence, the nanoscale determination of the barrier height represents a crucial requirement both for the optimisation of the state-of-the-art devices and for the demonstration of innovative ones. An innovative application of conductive atomic force microscopy (C-AFM) for high sensitivity (0.1 eV) and spatial resolution (~10 nm) determination of the barrier height of Schottky contacts on GaN and SiC has been recently demonstrated [2]. In Fig.2(a), a local I-V curve measured placing the nanometric C-AFM tip on a thin Pt layer deposited on GaN is reported and the estimated value of the local SB height is also indicated. By collecting a large array of local I-V curves, the histogram of the barrier height distribution for the laterally inhomogeneous Pt/GaN contact was obtained, as reported in Fig.2(b). The electrical behaviour of macroscopic Pt/GaN Schottky diodes could be explained both in terms of the measured nanoscale inhomogeneities of the SB and of the quality of the GaN material. In particular, the measured spread in the SB distribution is consistent with the observed temperature dependence of the ideality factor in the I-V curves measured on the diodes [3]. C-AFM was also applied to characterize the GaN epilayer electronic quality. In particular, the electrically active defects forming preferential conduction

paths through the GaN epilayer could be identified. Those defects affect both the reverse and forward bias behaviour of the diodes [4].
Finally, the quality of gate dielectrics on advanced wide-bandgap semiconductors (AlGaN/GaN, 3C-SiC) is not yet well assessed. C-AFM can be usefully applied to characterize the reliability of those dielectrics, performing a nanoscale correlation of current leakage with morphological features [5]. In particular, we investigated the reliability of thermally grown SiO_2 on 4H-SiC and on 3C-SiC, performing a nanoscale analysis of the breakdown events. This study allowed to clarify the role played by the material quality on the oxide reliability.

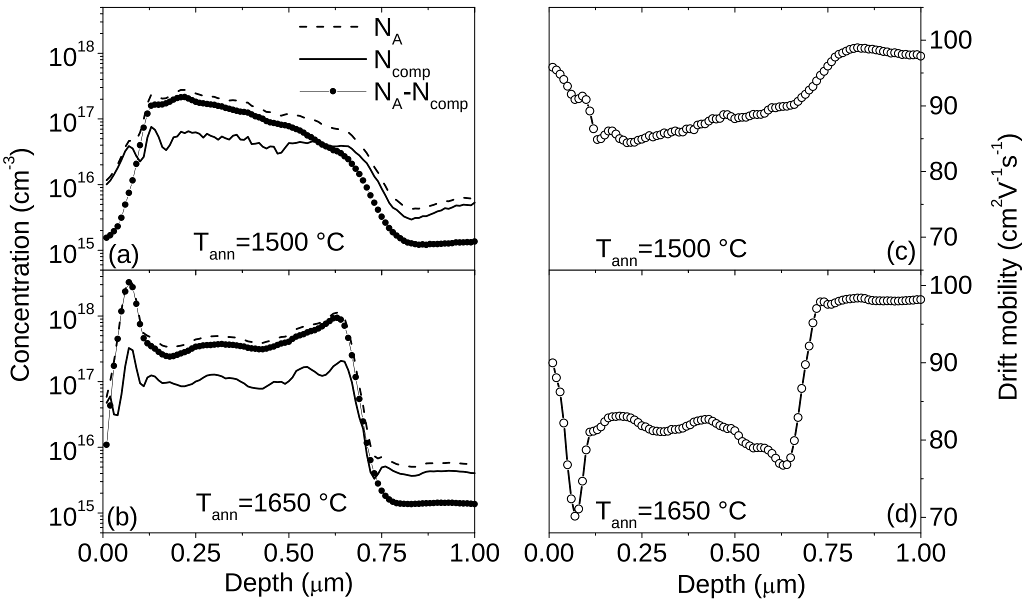

Fig. 1: Measured profiles of N_A, N_{comp} and of the net dopant concentration (N_A-N_{comp}) on Al implanted 4H-SiC after annealing at 1500 °C (a) and 1650 °C (b). The evaluated drift mobility profiles for the two annealing temperatures are reported in (c) and (d), respectively.

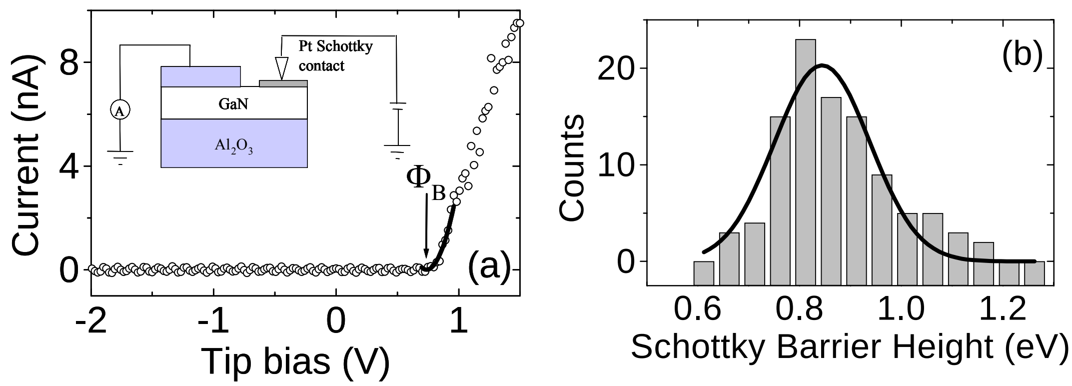

Fig. 2: (a) Local I-V curve measured placing the nanometric C-AFM tip on a thin Pt layer deposited on GaN; the estimated value of the local SB height is indicated. (b) Histogram of the barrier height distribution for the laterally inhomogeneous Pt/GaN contact.

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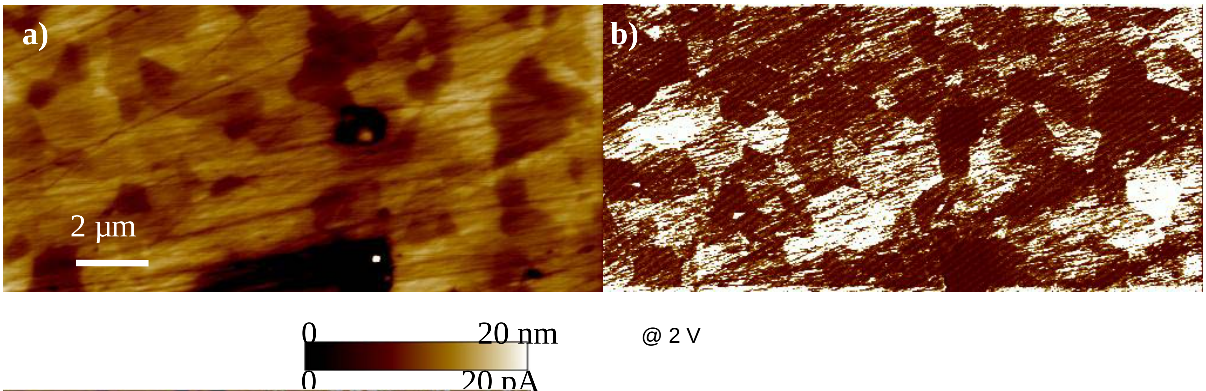
Sub-micrometer dielectric properties in advanced dielectrics for Rf technology

P. Fiorenza*, R. Lo Nigro, V. Raineri
CNR-IMM – Strada VIII n. 5, Zona Industriale, 95121 Catania, Italy
* Corresponding author: patrick.fiorenza@imm.cnr.it

This paper reports on the combination of scanning impedance microscopy (SIM) and conductive atomic force microscopy (C-AFM) to provide a valid characterization, with high lateral resolution, of inhomogeneous $BaTiO_3$ ceramics and in $CaCu_3Ti_4O_{12}$ (CCTO) single crystal, which are both dielectric materials for Rf application technologies. [1,2]
The microstructure and dielectric properties of Gadolinium-doped $BaTiO_3$ (BGTO) ceramics and of commercially available positive temperature coefficient of resistance (ptcr) $BaTiO_3$-based thermistor (BTO) have been studied. In both cases, the samples have been investigated in the 25 – 250 °C temperature range, so that the conduction mechanisms below and above the ferroelectric-paraelectric transition around the Curie temperature (around 130°C) have been studied.
For the BGTO sample, we provide evidence for phase-separation in two different phases comparing both the morphology (Fig. 1a) and the current map (Fig. 1b). The current map shows clearly that one phase is conducting and is associated with Gd-donor doping (electronic compensation) whereas the other is insulating and is presumably associated with some form of ionic compensation mechanism, either Gd-self compensation or A-site doping with the creation of Ti-site vacancies.
In the case of the BTO based thermistor (Fig. 2), the role of the grain core-shell and grain boundary interactions associated with the ptcr effect has been clarified and the spontaneous polarisation electric field has been estimated. These results have been compared with conventional Impedance Spectroscopy on the same materials, in order to obtain a more complete description and explanation of the macroscopic electrical properties.
The dependence of the depleted region width at the grain boundaries upon varying the sample temperature, below and above the Curie temperature (T_C), has been evaluated to get access to the mechanisms involved in the permittivity response at the transition temperature.
At temperatures below T_C ($T < 150°C$) the depleted insulating layer at the grain boundaries is 547 ± 1 nm thick as shown in the grains inside the highlighted circle (Fig. 2b and 2d). Increasing the temperature above T_C, the thickness of the depleted layer is reduced at 468 ± 1 nm (Fig 2f and 2h). This result can be discussed in terms of the internal local field (E_{Loc}) acting on the double Schottky barrier. In fact, below T_C the ferroelectric order produces an opposing internal field which acts as a screen to the applied field, while above T_C this screening effect is not present anymore and a forward polarization produces a “stronger” effect on the barrier width which is reduced. Thus, a reduction of the depleted region at the grain boundaries should be related to the disappearing of an inverse potential applied (due to the “ferroelectric order”) to the Schottky barrier at temperature below T_C. More information can be obtained by the current profiles across the grain and grain boundaries at different temperatures (Fig 3). A significant variation (about one order of magnitude) is present within the grains.
In the case of CCTO single crystal, both techniques can be employed to clarify the role of the inter- and sub-granular features in terms of conductive and insulating regions. The microstructure and the dielectric properties of CCTO single crystals have been studied and the evidence of internal barriers in CCTO single crystals has been provided. In particular, the imaging of domains, having different electrical characteristics (conductive and insulating properties), represents one important and possible explanation for the extrinsic origin of the giant dielectric response in CCTO.[3]



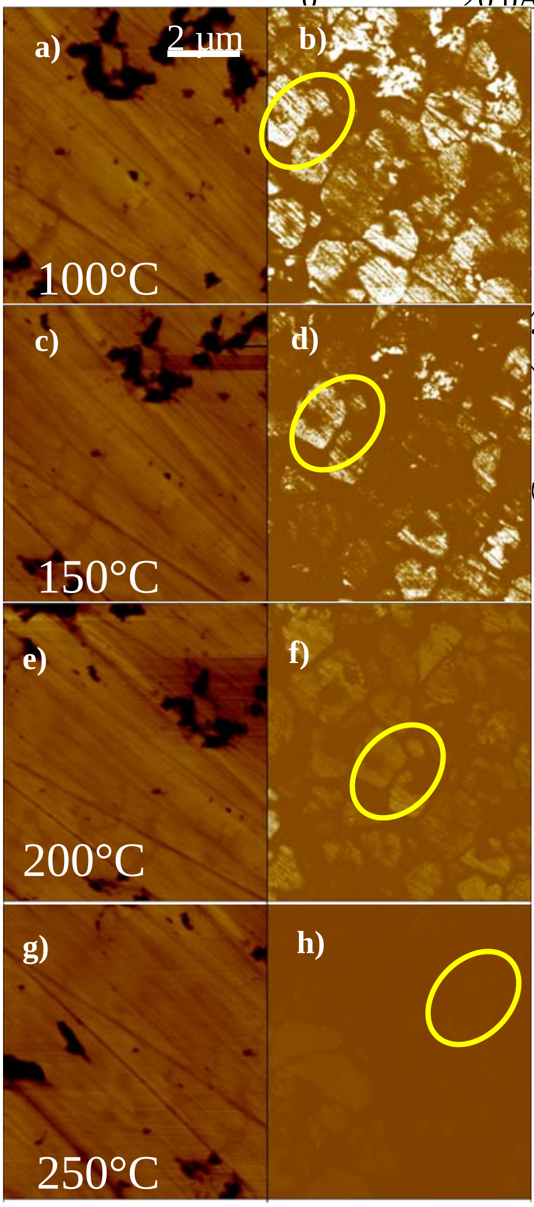


Fig.: 1: a) AFM morphology on BGTO. b) Current map acquired at 2 V shows clearly grains with higher conductivity.

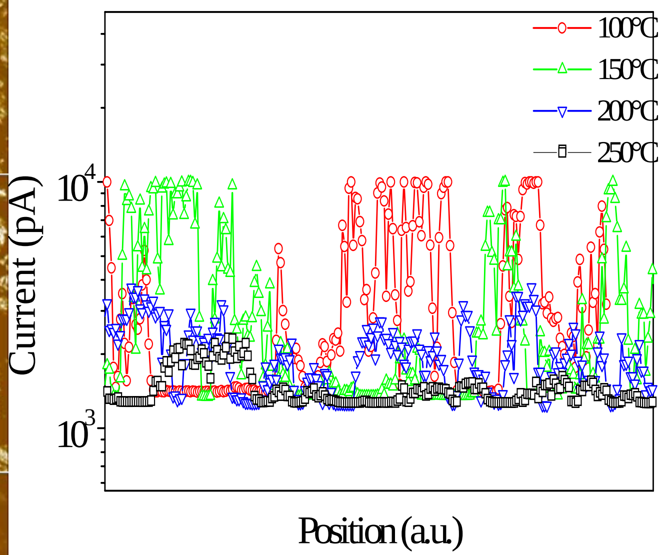


Fig.: 3: Current profiles across the grain and grain boundaries at different temperatures

Fig.: 2: a), c), e), g) AFM morphology images. b), d), f), h) Current map acquired at 4 V at 100°, 150°, 200° and 250° C respectively.

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Al^+ implanted 4H-SiC p^+n diodes: SIMS, C-V and DLTS characterizations

R. Nipoti[1*], F. Fabbri[2], F. Moscatelli[1], A. Poggi[1], A. Cavallini[3], A. Carnera[4]
[1]*CNR-IMM,via Gobetti 101, 40129 Bologna, Italy*
[2] *IMEM-CNR, viale Usberti 37/A, 43100 Parma, Italy*
[3] *Phods Lab, Department of Physics, University of Bologna, and CNISM, Bologna, Italy*
[4]*Department of Physics, University of Padova, Italy*
[*]Corresponding author: nipoti@bo.imm.cnr.it

In a previous study, the measured forward and switching characteristics of Al^+ implanted 4H-SiC p^+/n diodes were simulated assuming that the implanted Al^+ ions were 100% in substitution positions and partially ionized and that the diode structure was P-i-N like [1]. The "intrinsic like" region between the p^+ and the n sides of these Al^+ implanted junctions was justified by the presence of a slow degrading tail on the Al depth profile towards the bulk material. It is known that ion straggling is not enough for justifying such a long degrading tail, also an high probability of unintended ion channelling trajectories during implantation in SiC have to be admitted [2]. Depending on the electrical activation and the bias value, such a doping tail can be included as a part or entirely in the space charge region of the implanted bipolar SiC junction. With the aim to gain a thorough picture of the interface layer between the p^+ implanted depth and the n-type epilayer material a set of Al^+ implanted p^+n 4H-SiC diodes have been characterized by Secondary Ion Mass Spectroscopy (SIMS), capacitance-voltage (C-V) and Deep Level Transient Spectroscopy (DLTS).

Al^+ implanted 4H-SiC p^+/n diodes have been fabricated on 8° off-axis n-type epitaxial 4H-SiC material. The epilayer was compensated with Al and B for obtaining an n-type conduction of 1.6×10^{14} cm^{-3}. The Al^+ implanted p^+ emitters of these diodes were circular with diameter in the range 800 – 1000 μm. A fraction of these emitters were surrounded by an Al^+ implanted p^- zone of 240 μm forming a Junction Termination Extension (JTE). Both p^+ and p^- implantation processes were performed at 400°C. An inductively heated furnace with a heating ramp-up of 40°C/s was used for post implantation annealing at 1600°C for 5 min without cap and in a high purity Ar atmosphere. The as-implanted Al depth profiles on p^+ and p^- areas have been measured by SIMS and are shown in Fig.1. Literature and our direct experience agree on the fact that implanted Al atoms are immobile during post implantation annealing for that Al profiles after post implantation annealing can be assumed equal to those of Fig. 1. Ohmic contacts on the p^+ emitters and on the n^+ base have been made of Al/Ti and of Ni alloys, respectively. Al/Ti Schottky diodes have been also fabricated on un-implanted areas of the same 4H-SiC wafer.

Three different device structures have been characterized by C-V and DLTS: diodes with JTE (set A), diodes without a periphery termination (set B), and Schottky diodes (set C). C-V measurements at room temperature (RT) and under reverse bias up to 10 V show that a linear trend holds on between the square of the depleted SiC thicknesses and the bias values for all the devices. The apparent carrier depth profiles over the maximum depleted thickness computed by C-V measurement data are flat and equal to about 1.5×10^{14} cm^{-3} for all the devices. Taking into account the depth profiles of Fig. 1 and the fact that the maximum depleted thickness can lay at different depths in samples A, B and C, an equal apparent carrier concentration profiles in each device type allow us to hypothesize that in implanted diodes the space charge region extends mainly on the n-side of the junction that has a doping level coincident with that of the original epitaxial 4H-SiC material. During DLTS measurements a constant reverse bias of 10 V with a bias filling pulse in the range -7 – 0 V and a SULA transient spectrometer in the temperature range 80 – 500K have been used. For each diode set at RT this bias configuration corresponds to a majority carrier injection from the n-side neutral region. The freezing out of the n-type Nitrogen (N) doping limits the minimum

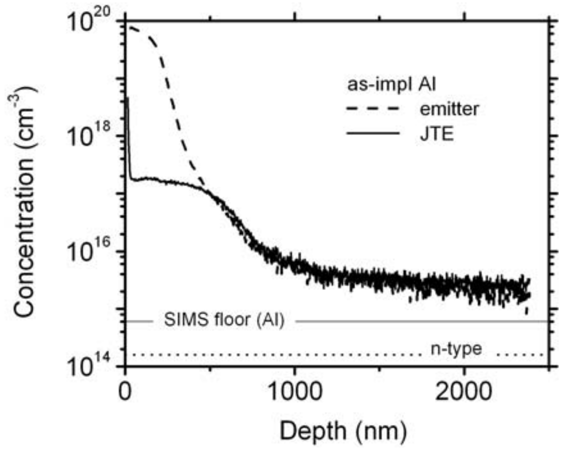

Fig. 1. SIMS profiles of as-implanted Al in emitter and JTE areas. Measurement floor and n-type concentration in the epitaxial 4H-SiC are also shown for comparison.

measurement temperature at 80 K. Fig. 2 shows typical DLTS spectra that have been recorded at every bias filling pulse value for each set of diodes. The set C (Schottky diodes) spectra have peaks of a single sign that correspond to majority carrier traps: electrons in these samples. But sets A and B (implanted diodes) spectra have peaks of both signs, which indicate the presence of both minority and majority carrier traps. More precisely, in Fig. 2 the comparison between Schottky (set C) and implanted (sets A and B) diodes shows all the diodes have the same electron traps, these are SE1, SE2 and SE3, but implanted diodes have two more majority carrier traps SE3* and SE4. Moreover, only the spectra of implanted diodes have features of minority traps, these are peaks SH1* and SH1. With the increasing of the bias filling pulse from -7 to 0 V peak SH1* is almost constant while peak SH1 increases. The feature of a minority carrier trap in DLTS spectra intended for measuring majority carrier traps has been measured also in the case of Si and GaAs diodes [3] and of B^+, Al^+ and Ga^+ 6H-SiC implanted p^+n junctions [4-6]. This is the first time such DLTS spectra have been measured on Al^+ implanted p^+n 4H-SiC junctions. A minority carrier trap peak in a DLTS spectra intended for measuring majority carrier traps has been explained in ref.[3] as a signal arising from the communication between a deep level trap and free-carriers tails in the depletion region. Trap energy levels and cross sections computed from the Arrhenius plots of the DLTS peaks of Fig. 2 are shown in Table 1. Taking inspiration from these values and from the literature, a defect attribution to each DLTS peak of Fig. 2 is proposed in Table 1.

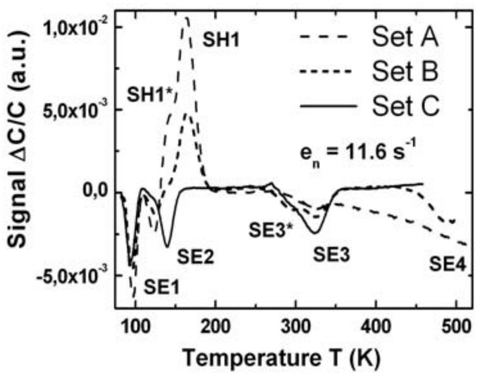

Fig. 2. Typical DLTS spectra of diodes with JTE (set A), diodes without termination extension (set B) and Schottky diodes (set C).

Table 1. Energy level, cross section and attribution of the DLTS peaks in Fig.2.

	Energy (eV)	Cross-section (cm^{-2})	Attribution
SE1	0.19	3×10^{-14}	Ti acceptor
SE2	0.22	2.5×10^{-14}	Single plain SF
SH1*	0.24	7×10^{-16}	Al Doping acceptor
SH1	0.34	5×10^{-14}	D1 pseudo-donor
SE3*	0.53	7×10^{-16}	Z_2 (0/+)
SE3	0.66	3.5×10^{-15}	Z_1/Z_2 (Vc+Vsi)
SE4*	1.04	6.3×10^{-14}	Al(int)-C(int)
SE4	1.17	1×10^{-13}	EH5 (Vc+Vsi)

The SH and SE energy levels are intended from the valence and conduction band edge, respectively.

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SiC technology for power devices fabrication in a standard industrial environment

M. Saggio[1*], F. Giannazzo[2], F. Roccaforte[2], A. Ruggiero[1], E. Zanetti[1],
[1]*STMicrolectronics IMS R&D, Stradale Primosole 50, 95121 Catania, Italy*
[2]*CNR IMM, Strada VIII n.5, Zona Industriale, 95121 Catania, Italy*
[*] Corresponding author: mario.saggio@st.com

Activity on Silicon Carbide (SiC) Power Devices has to overcome many issues related to material peculiarity. Wafer size, material hardness, crystal complexity, surface reactivity [1] put many issues on device fabrication to be solved. Nevertheless SiC, for its own physical characteristics, still remains the key candidate to substitute Silicon for many applications in power structures of next generation [2]. The passage from a niche market where SiC ruggedness to harsh environment is requested to a mass market amplifies workability issues but, on the other side, increases focus on SiC world, allowing to step up a positive feedback that after an increase of fabricated devices and processed wafers will help to increase industrial solutions and, as a consequence, a material cost reduction. Today device manufacturing cost is a small percentage of final device cost, the largest part goes to raw material supplier. A larger market penetration will drive to a better balance in costs' scale.
In order to enlarge SiC applications, R&D ST Department, together with CNR-IMM lab, is focused to develop new technologies for high voltage power rectifiers and switches in Silicon Carbide. Targeted applications range from industrial to automotive to consumer and to energy conversion. In any case efficiency increase is the driving force.
Fig. 1 shows, in the plane with request for many applications in terms of conduction and blocking capability, the area where SiC devices can play a key role. In order to allow SiC devices to really cover this area in a valuable way, giving advantages to power semiconductor industry from manufacturers to end users, it has to be demonstrated the quality of process in this material and the reliability of obtained devices in end user application, in operative conditions.
In this landscape a full knowledge of device elementary bricks is the fundamental resources to integrate new structures for power devices. New architectural solutions need to overcome intrinsic material difficulties and limits as inexistent dopant diffusion (in industrial available process temperature ranges), low activation ratio, low surface carrier mobility.
Device integration has to give the same result on the whole surface of a wafer with an acceptable variation from the center to the edge and has to guarantee repeatability from wafer to wafer and, in a production, from one lot to another one. An efficient process control is the basis to allow such a result and allow device manufacturing with a good process yield.
Limiting issues to reach such a target are raw material quality and process equipment availability. SiC wafer quality in last years has had a very big enhancement nevertheless lattice defects (mainly micropipes) remain the Yield loss major cause in produced High Voltage SiC diodes. Future technologies will drive the demand to reduce other stable defects (mainly dislocations) in order to fabricate devices on a mature material having zero impact on process Yield. Material size is the first root cause of process equipment lack. The workability of commercial wafers having 75 or 100mm diameter is in many case limited by the absence of new high performance equipments, today equipment supplier are focused to 200/300 mm wafers for Si and hardly they look to our small wafers. The current solution is the downgrade of previous generation equipments or, when possible, to adapt large diameter (typically 150mm) process to smaller size wafers. The other reason limiting SiC workability is SiC peculiarity itself. The dopant activation temperature is much higher respect to Si one and in many cases equipments running this particular processes are still not "enough" industrial and too close to research lab approach where they were formerly studied. Ion implantation is another relevant issue. In order to limit damage introduced and promote dopant activation, it

has to be performed maintaining the target temperature between 500 and 1000 °C. This, together with small wafer diameter, goes in the opposite direction respect to Si ion implantation where target has to be chilled, so that high temperature commercially ion implanter are not available till now and, once more, not industrial solutions limiting equipment throughput are put in place.
In this scenario semiconductor industries have to move working with a very promising material but with some relevant issues to face. The goal is fabrication of power devices able to overcome the reliability trials simulating device real life in the application. This guarantees quality standard to the final user and respect the agreement between manufactures and customers. STMicroelectronics takes advantage in this on a more than 30 years experience on Silicon devices which can offer to Silicon Carbide market a complete chain from device design to application study going through device characterization allowing a step forward toward the full maturity of the market.
Today, in Catania 150mm front, end line a *mature* production of 600V diodes is running [3]. These diodes are in ST portfolio and promoted to mass market application for power conversion. Together with this STM 1200V diodes are close to be available in the market, but key activity and focus is on SiC power switch and an advanced R&D program is active to develop High Voltage MOSFET technology ranging from 900V to 1700V. The goal of MOSFET activity is to develop a technology ensuring a strong stability of electrical parameters being reliable in a wide range of applications. In order to reach the desired reliability conditions heavy trials are carried on to prevent any failure in the field, during device lifetime. The challenge is important also in terms of characteristics because improved structures on Si devices overcome Si ideal limit [2] and they are reducing the nominal gap between Si and SiC power devices. This is shown in Fig. 2 where together with “theoretical” limit of Si and SiC power devices are reported on resistance vs. Breakdown Voltage of new Si Superjunction devices (MD5[4]) or Si IGBTs.

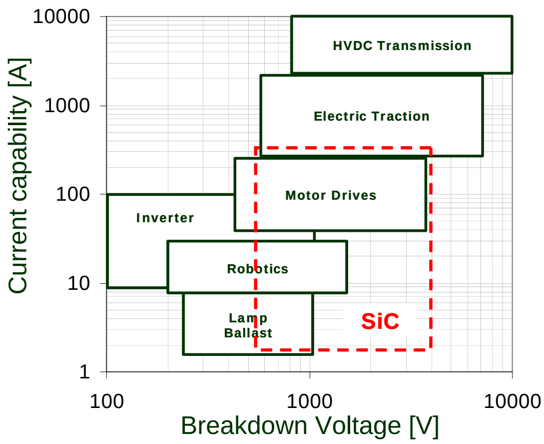

Fig. 1: Applications for Power Devices in Si and SiC.

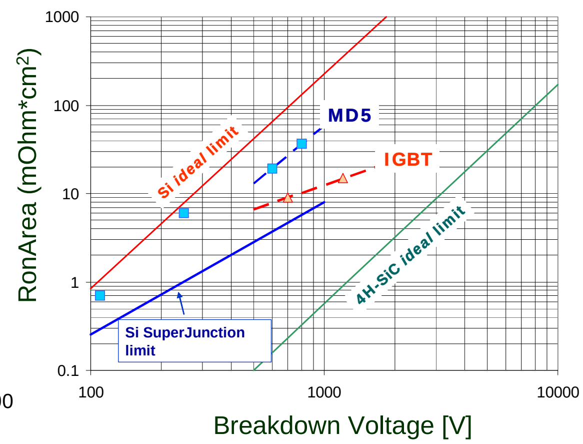

Fig. 2: From Si to SiC. Trade-off curves of R_{on} vs V_B for power devices

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A step toward fully integrated monolithic driver for 1.2 kV-3/5kV SiC-BJT high temperature applications

D. Tournier*, P. Bevilacqua, P. Brosselard, D. Planson, B. Allard
Ampere (UMR CNRS 5005), INSA de Lyon, Bât. Léonard de Vinci, 21 Avenue Jean Capelle, 69621 Villeurbanne cedex, France
* Corresponding author: dominique.tournier@insa-lyon.fr

Looking back to the development of inverters using SiC switches, it appears that SiC devices do not behave like their silicon counterparts. Their ability to operate at high temperature makes them attractive. Developing drivers suitable for 200˚C operation is not straightforward. In a perspective of high integration and large power density, it is wise to consider a monolithic integration of the driver parts for the sake of reliability. Silicon is not suitable for high ambient temperature; silicon-on-insulator offers better performances and presents industrial perspectives. Whatever the central question of the system schematic remains. The paper focuses on a SiC BJT driver, with a work objective of two fold: validate the SiC BJT driver schematic and deliver the specifications for the integration of SOI CMOS of the driver for SiC-BJT high temperature application. Indeed, BJT-driver processes logical orders from outside, drives adequately the BJT to turn it on and off, monitors the turn-off and turn-on state of the device, and acts accordingly to prevent failure. Particularly the driver must anticipate and correct the evolution of the SiC BJT performances under high temperature conditions.
Several investigation teams are currently working on the development of high temperature power switch, sensors and packaging issues. Silicon devices have reached their theoretical limits. SOI technology giving a margin to temperature operation of up to 200°C [1]. SiC devices are pushing up both high temperature and high voltage silicon limits, as wide band gap devices (SiC and GaN) are promising solutions for the fabrication of high temperature switches [1-5]. However, only power side devices have been developed so far and both driver and signal conditioning issues are not specifically addressed. Drivers are usually based on silicon discrete or integrated devices, and system architectures are constrained by thermal limitations. Amplification and drivers still remains a major point to solve for high temperature normally-on and normally-off devices. Up to now, the conventional solution was to consider a thermal adaptation path between high temperature and low temperature sides (Fig. 1). In order to reduce thermal stress for high temperature applications, and to match severe operating conditions (as high as 500 ˚ C), an new thermal path configuration must be foreseen (Fig. 2). The conception of such a new architecture implies to identify limiting key points of each elements of the energy conversion chain : from control to driving block and high voltage power switches. Issues for high temperature application are to address at least the following critical points making possible to reduce system EMI susceptibility, cooling effort, impacting directly the efficiency :

- high temperature power switch,
- high temperature logic control block (amplification for drivers),
- high temperature packaging.

High temperature integrated circuit (MOSFET amplifier operating at 300°C [6-9]) have been successfully fabricated. Since then, several high temperature sensors, switch and converters have been designed [10-14]. A monolithically integrated power converter has been presented [15], however this work addresses only the high side SiC stage of JFET driver and do not include protection feature or dead-time control. Even if for highest temperature range (>300°C) no mature technology addressing both device and system is right now commercially available, it is reasonable to define new converters topologies based on
SOI in a first step. Prior to driver design work, it is wise to consider the specificities of

normally-off devices to design an appropriate gate driver. Indeed, the knowledge of power switch gate equivalent impedance, transient gate supply current, reverse and forward characteristics and temperature impact on all BJT-parameters is mandatory to design a reliable high temperature gate driver.
In order to quantify this benefits, both static and dynamic electrical characterization of 1.2kV SiC-BJTs (from Transic) have been investigated. Static SiC-BJT characterizations have been performed, to check the temperature impact on BJT gain among others parameters. BJTs on-resistance is increased by a factor of 1.4 for a temperature increase of 100°C while the current gain (Ic/Ib) decreases by a factor 1.43 (33 to 24). One can conclude from Fig. 3, that for the BJT-nominal current (In=6A), the maximum gain corresponds to a base current in the range of 250mA < Ib < 300mA. No dynamic adaptation of the base current would be necessary on the driver side. The driver topology is thus strongly simplified since no temperature sensing and correction of side-effects is required. Based on previous BJT characteristics, a discrete driver version has been designed, optimized and fabricated. The BJT driver topology (to be integrated using SOI technology) is presented in Fig. 4. The circuit can be partitioned into several functional blocks : positive and negative isolated auxiliary power supplies, short circuit protection by V_{CE} (sat) monitoring, cross conduction protection. Switching waveforms (Fig. 5) at optimal driving conditions shows satisfying performances of driver/SiC-BJT association. A short over-current applied on the base allows fast turn-on (Fig. 5-right). Driver turn-off block permits V_{CE} over-voltage limitation as inferred from Fig. 5-left (ΔV_{CE}=90 V). Minor impact of temperature on switching performance has been measured (Fig. 6). Switching energy losses remains almost constant up to 200°C as inferred from Fig. 7-left, as well as buck-converter efficiency (η=0.9) versus switching frequency (Fig. 7-right).
This paper focuses on a preliminary analysis of the driver functions for a SiC BJT, anticipating the behavior of the device and the change in behavior at high temperature. Fully integrated SiC driver might be the ultimate high temperature option, however, whatever material is chosen, the central question of the system schematic remains. Functional blocks to be monolithically integrated have been successfully tested, SiC-BJT operating at high temperature. For high voltages (3kV and above), BJTs offers better performances than JFETs, with similar switching performances (20 ns < t_{ON-OFF} < 200 ns), energy losses. For high voltage applications (V> 1.2kV), bipolar devices are to be preferred to JFETs as their characteristics are less dependent on temperature.

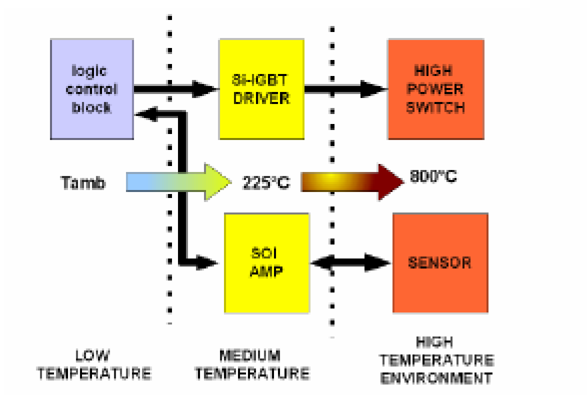

Fig 1: Usual "high temperature" converters topology using SOI technology for medium temperature range

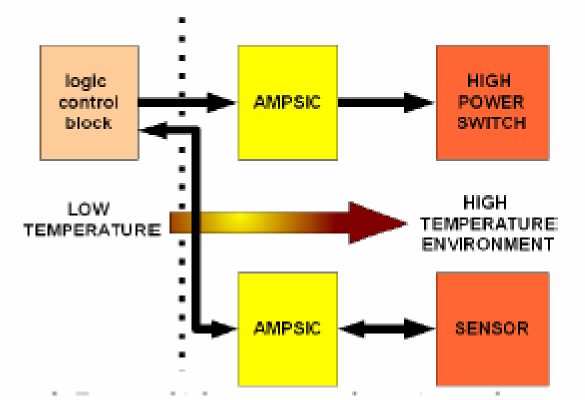

Fig 2: Proposed high temperature converters topology

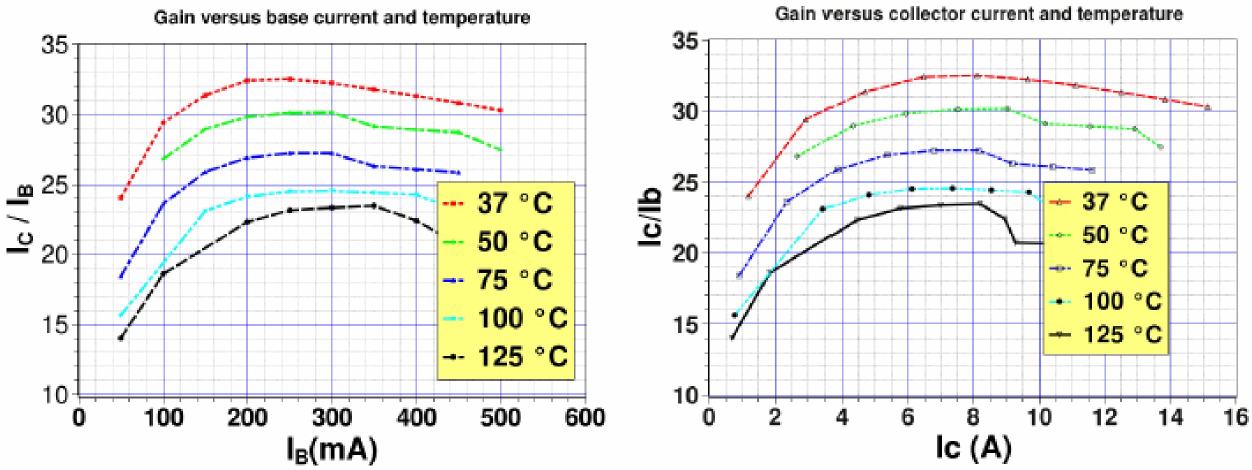

Fig 3: Current gain versus, base current (left), collector current (right), depending on temperature.

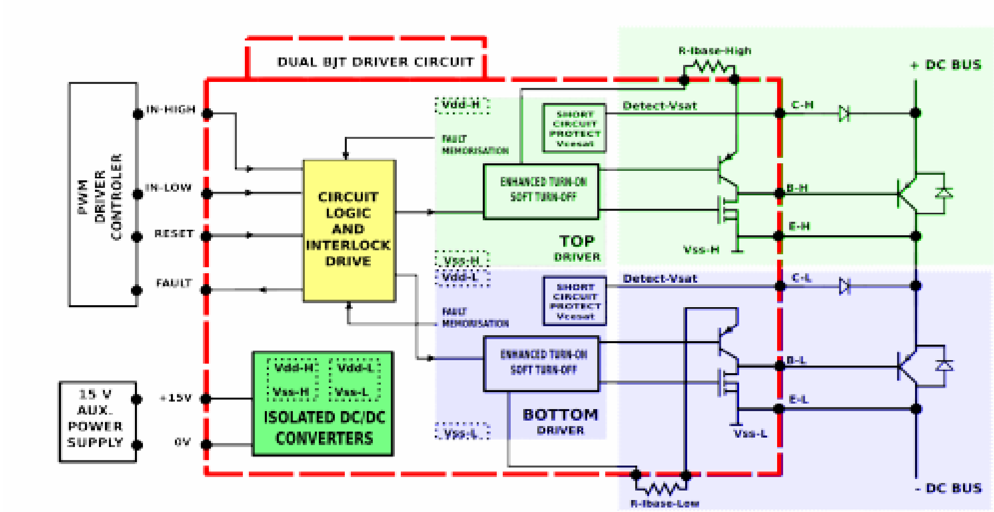

Fig 4: Fabricated discrete BJT driver topology (dashed rectangle to be integrated using SOI technology).

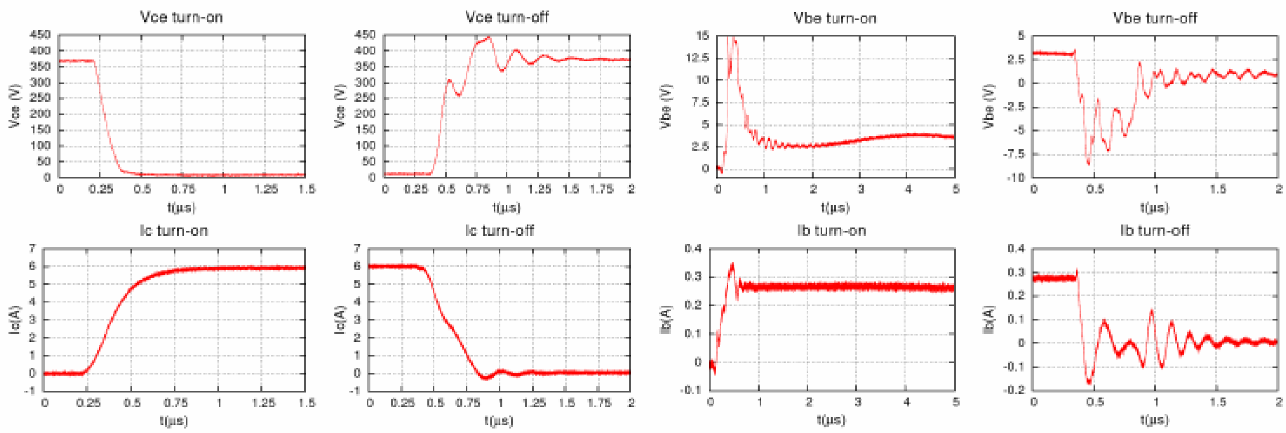

Fig. 5: Switching waveform : collector (left), base (right) using discrete driver.

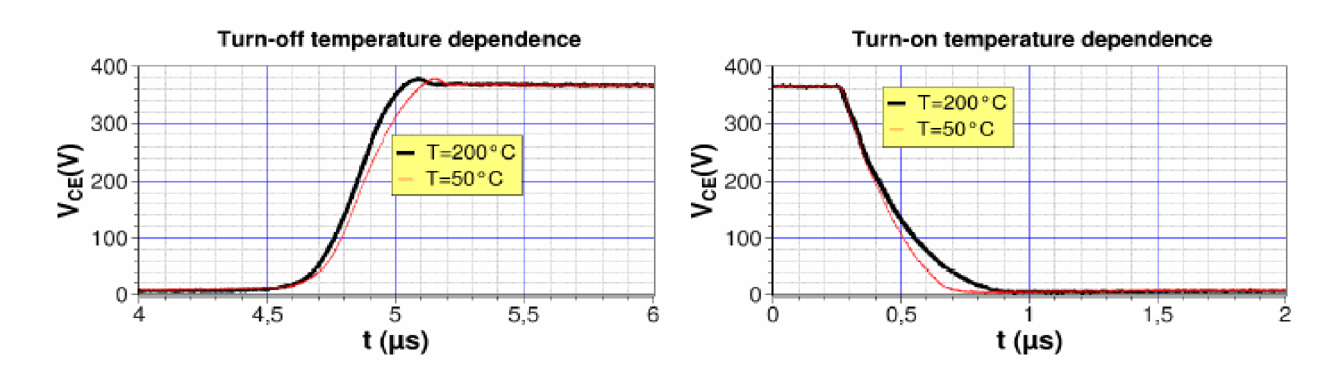

Fig. 6: Turn-off (left) and turn-on (right) dependence on temperature (50°C and 200°C).

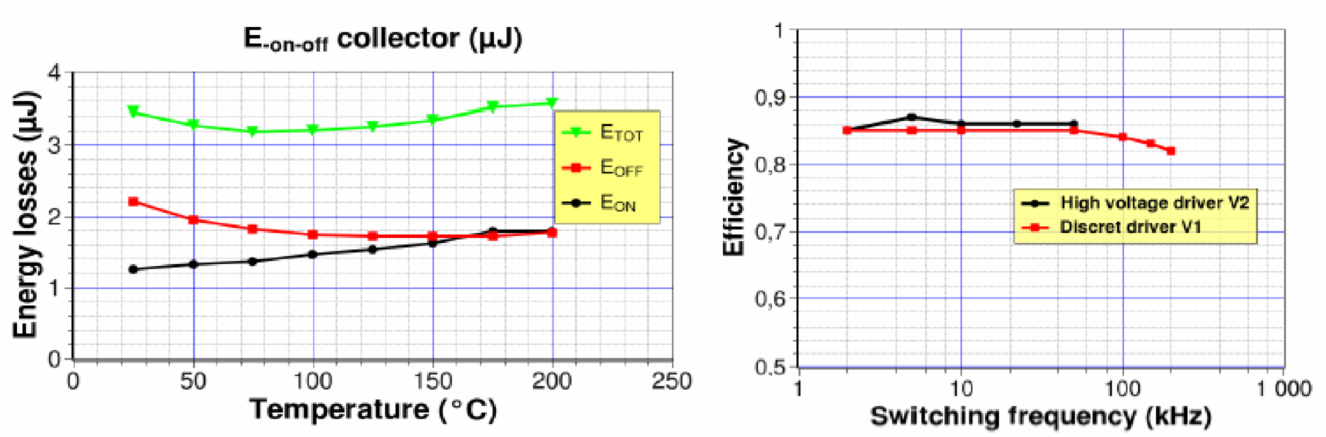

Fig. 7: Losses versus temperature (left), efficiency versus switching frequency (right).

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Towards high power Schottky diodes in GaN: main challenges

F. Iucolano[1*], F. Roccaforte[1], F. Giannazzo[1], S. Di Franco[1], V. Puglisi[2], V. Raineri[1]
[1] *CNR-IMM, Strada VIII n.5, Zona Industriale, 95121 Catania - Italy*
[2] *ST-Microelectronics, Stradale Primosole 50, 95121 Catania - Italy*
[*] Corresponding author: ferdinando.iucolano@imm.cnr.it

Due to its outstanding properties (wide band gap, high electrical field,…) Gallium Nitride (GaN) is potentially competitive to Silicon Carbide (SiC) for the fabrication of high-power Schottky diodes, as it can theoretically achieve the same performances of SiC, with lower material costs. However, GaN-based power diodes technology is limited with respect to SiC, mainly due to the lack of high quality free-standing GaN substrates. Moreover, the lack of lattice matched substrates with GaN leads to high densities of dislocations in the epitaxial GaN films, typically in the order of 10^8–10^{10} cm^2. The presence of these defects represents a huge limitation for the devices performances and reliability. Besides the material quality, other specific crucial topics related to GaN-based devices fabrication are the formation of ideal and reliable Schottky contacts, the comprehension of the electrical activation mechanisms of guard-ring ion-implanted layers, and their influence on the leakage current.
In this work, the most critical concerns related to GaN Schottky diodes for high-voltage are discussed. In particular, to understand the deviations from the ideal behaviour of Schottky contacts, a nanoscale study of Schottky barriers was carried out by means of conductive atomic force microscopy (C-AFM) measurements, combined with conventional current-voltage (I-V) characterization of the diodes. Furthermore, since an optimal diode layout requires efficient edge terminations to increase the breakdown voltage, the use of Mg-implanted guard-rings in GaN Schottky diodes is also discussed.
Lateral Schottky diodes were fabricated on n-type (~ 1×10^{16}cm^{-3}) GaN epitaxial layers grown on Al_2O_3 substrates. A ring-shaped Ohmic contact was formed by deposition of Ti/Al/Ni/Au multilayer and subsequently annealing in Ar at 750°C [1,2]. The circular Schottky contact was formed by sputtering Pt/Au or Ni/Au bilayers, followed by a post-deposition annealing at 400°C to improve the contact properties [3]. The I-V characteristics of the diodes were measured at different temperatures, ranging between 25 °C and 175 °C. The nanoscale electrical properties of the barrier were monitored by local I-V measurements, performed using a DI-3100 atomic force microscope (AFM) with a biased conductive tip [4]. A detailed description of the experimental set-up and of the sample preparation is given elsewhere [3].
Local I-V measurements on Pt/GaN Schottky contacts annealed at 400°C were carried out by means a C-AFM, determining the local Schottky barrier height with a spatial resolution of 10-20nm [4]. The statistical distribution of the barrier height values was determined scanning the biased tip over a 5×5 μm^2 area. A Gaussian distribution with a mean value of 0.84eV and a standard deviation σ_Φ= 0.11eV was obtained, in agreement, with the formation of a laterally inhomogeneous barrier. The barrier height distribution width can be correlated to the temperature dependence of the ideality factor of the macroscopic Schottky diodes through [3,5]: $n = 1 + \frac{q\sigma_\Phi^2}{3kTV_{bb}}$, where V_{bb} is the band bending. The temperature dependence of the ideality factor *n*, determined from the I-V characteristics of Schottky diodes, and the theoretical curve, obtained substituting in the previous expression the value of σ_Φ determined from the nanoscale measurements, are reported in Fig. 1. As can be seen, the experimental data on macroscopic diodes are very well described by the theoretical behavior obtained from the nanoscale analysis of the local barrier distribution [3,6]. The barrier inhomogeneity may find its physical origin in material quality issues. In fact, studying the morphological and electrical properties of the bare GaN surface we demonstrated that the presence of

dislocations is responsible for highly localized leakage current paths and for the non-ideal behavior of the macroscopic contacts [6].

Another challenging aspect correlated to GaN power devices is the possibility to fabricate efficient edge terminations to increase the device breakdown voltage. Although edge terminations for GaN diodes can be formed by Mg-implanted guard-rings, the activation of the implanted species and the effects on the device leakage current were not investigated in detail. In this work, annealing at high temperatures (>1100°C) were performed to obtain the activation of Mg-implanted ions (50keV, 5×10^{14} ions/cm^2) [7]. Although the surface was protected by a SiO_2 cap layer during annealing and the morphology was preserved, a degradation of the electrical behaviour of Schottky contacts was observed. In particular, the temperature dependence of the reverse characteristics of Schottky contacts allowed to demonstrate the predominance of one dimensional variable-range hopping conduction when the contact is fabricated on a high temperature annealed surface [8]. Frequency dependent capacitance-voltage measurements allowed to ascribe this behaviour to a high density of interface states at the metal/GaN interface in the high-temperature annealed samples [8].

Fig. 2 compares the electrical characteristics of Schottky diodes with and without an implanted termination. Clearly, in the absence of a post-implantation annealing, a Mg guard-ring can be beneficial to reduce the leakage current, acting as a highly resistive layer that limit the electric field crowding at the device corners.

In summary, a nanoscale study of the Schottky contacts on GaN demonstrated the formation of a laterally inhomogenous barrier, that in turn can be correlated to the presence of a high density of dislocations. Beyond this aspect, for power devices applications, Mg-implanted guard-ring can be used to improve the reverse characteristics, even if an optimal choice of the post-implantation annealing conditions is required to avoid a high density of interface states at the metal/GaN interface.

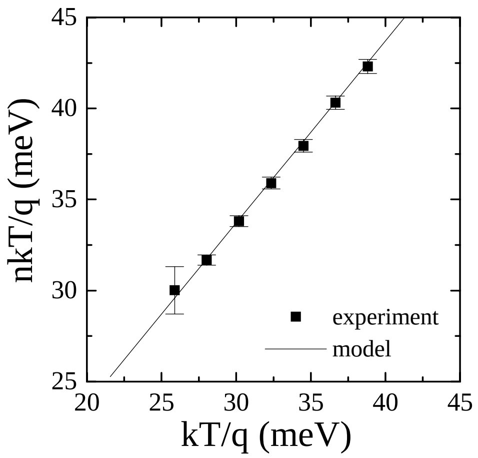

Fig. 1: Plot of *nkT/q* as a function of *kT/q* of macroscopic Au/Pt/GaN Schottky diodes and the theoretical curve obtained from the nanoscale barrier height distribution.

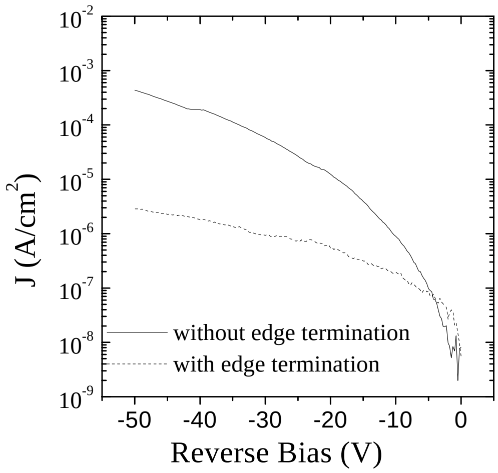

Fig. 2: Reverse characteristics of Ni/Au Schottky diodes with and without non-annealed Mg-implanted guard ring.

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Planar Schottky diodes made on gallium nitride (GaN) grown on sapphire: Impact of the process parameters.

O. Menard[1,2*], F. Cayrel[1], E. Collard[2], D. Alquier[1]

[1] *Université de Tours, LMP (Laboratoire de Microélectronique de Puissance), 16 Rue Pierre et Marie Curie, 37071 TOURS France*

[2] *STMicroelectronics, 16 Rue Pierre et Marie Curie, 37071 TOURS France*

[*] Corresponding author: olivier.menard@st.com

In order to realize power devices operating at higher switching speed, temperature and power level than the conventional Si devices, new performing materials are required. Among them, GaN is a promising candidate due to its intrinsic properties such as ~~a~~ wide band gap (~3.4eV at room temperature), high saturation velocity ($3x10^7$ cm/s, higher than for SiC) and also high critical electric field ($\geq 4x10^6$V/cm) and has led to an expanding research topic [1-3].

Among the numerous parameters requested to realize a complete Schottky diode on GaN, ohmic and Schottky contacts are two critical steps. In previous work, a set of process parameters leading to a good ohmic contact have been extracted [4]. The aim of this paper is to study the quality of the Ni Schottky contacts realized by DC Magnetron sputtering. To do so, two structures were implemented on N-type GaN grown on sapphire substrates. First, a “Schottky to Schottky” structure is realized through standard photolithography process that allows us to study the reverse leakage current depending on process parameters such as Ni layer thickness, contact annealing temperature or duration as well as presence of a PVD SiO_2 or TEOS insulation step. This simple structure allows us to discriminate easily various process parameters with only one masking level structure.

Then, Schottky Barrier Diodes (SBD) with Ni and Ti/Al, respectively for Schottky and ohmic contacts, were realized. Ti(50nm)/Al(200nm) bi-layer contacts were sputtered and annealed at 650°C during 60s [4]. Diodes were patterned through lift off or standard photolithography processes. The influence of parameters such as the presence of the insulation step or the annealing conditions of Schottky contact on the diode’s characteristics was then investigated.

Current density versus Voltage (J-V) measurements on “Schottky to Schottky” structures, presented on fig. 1 for a 30min furnace annealing at 400°C, evidences the impact of the insulation step presence. For a 300nm Ni thickness, always giving the best J values, PVD oxide largely degrades current density values compared to structures with TEOS or without insulation step. J-V characterizations, on fig. 2, reveal that the lowest leakage current is obtained when sample is annealed at 450°C during 3min (RTA). Then, J-V comparison between SBD made by lift-off and wet etch photolithography, represented on fig.3, shows that photolithography process using wet etching is more convenient to achieve higher barrier heights and lower ideality factors, which are respectively rising from 0.64eV to 0.86eV and decreasing from 3.03 to 1.13.

Finally, this work demonstrate that promising GaN SBD results with an ideality factor around 1.13 and a barrier height of 0.87eV (see fig. 4) and low leakage current can be achieved. Furthermore, those values can probably be improved. Indeed, guard rings and ohmic contacts, done by ion implantation, are very promising issues.

The authors would like to thank Velox Semiconductor Corporation for providing the MOCVD grown GaN samples and Pr. C. Brylinski at LMI (Lyon) for valuable discussions. This work was financially supported by OSEO project “G^2REC”.

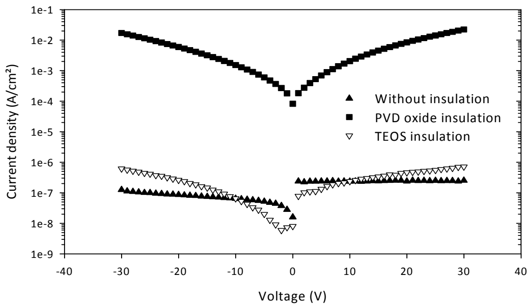

Fig. 1: Comparison of J(V) on “Schottky to Schottky” structures with or without an insulation step. (Furnace annealed at 400°C during 30min).

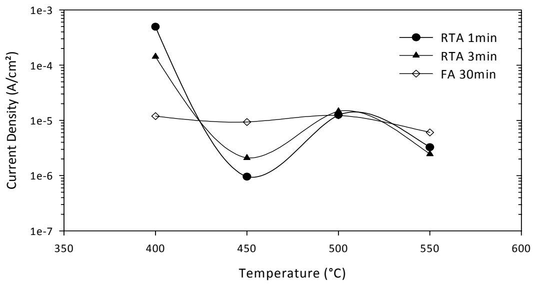

Fig. 2: Current density measured at 30V on non insulated “Schottky to Schottky structures” for different annealing durations, as a function of annealing temperature.

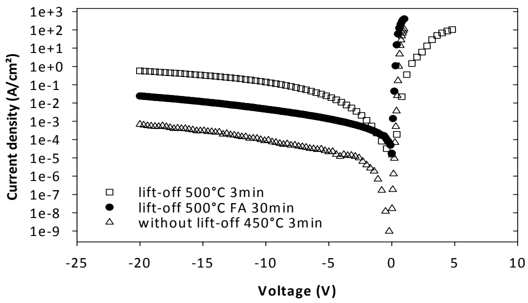

Fig. 3: Best /J/-V characteristics for SBD made by lift-off or using standard photolithography process at various temperature.

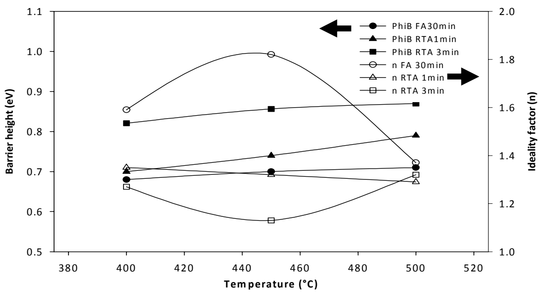

Fig. 4: Barrier heights (left-axis) and ideality factors (right-axis) for non lift-off SBD annealed 3min in RTA.

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The heterojunction properties of a novel Ge/SiC semiconductor structure.

P. M. Gammon[1*], A. Pérez-Tomás[2], M. R. Jennings[1], G. J. Roberts[1], V. A. Shah[3], J. A. Covington[1], and P. A. Mawby[1].
[1]*School of Engineering, University of Warwick, Coventry CV4 7AL, United Kingdom*
[2]*Centre Nacional de Microelectrónica, Campus UAB, 08193 Barcelona, Spain*
[3]*Department of Physics, University of Warwick, Coventry CV4 7AL, United Kingdom*
[*] Corresponding author: P.M.Gammon@Warwick.ac.uk

In this paper we investigate the physical and electrical properties of Germanium (Ge) thin films grown on 4H Silicon Carbide by molecular beam epitaxy (MBE), evaluating the effect of deposition temperature and Ge doping using x-ray diffraction, atomic force microscopy, capacitance-voltage and current-voltage techniques.
SiC schottky diodes take advantage of the material's superior reverse breakdown voltage when compared to Silicon (Si) [1]. However, the high concentration of interface traps at the SiC/SiO_2 interface reduces the material's already low channel mobility [2]. Therefore, a Ge/SiC heterojunction solution becomes an attractive prospect, whereby the Ge forms the control region. With a well established Ge-High K dielectric technology [3], a carbon-free oxide would exist, leaving a channel-region with a mobility approximately four times that of SiC.
An n-type (0001) Si face, 4° off axis, 4H-SiC wafer was purchased from Cree Inc with a 10 µm, lightly n-type doped ($N_{D,SiC} = 1.4\times10^{15}$ cm^{-3}), epitaxial layer. Germanium films were deposited using a V100S MBE system. Prior to deposition, the wafer was cleaned using a standard RCA wafer cleaning process. N-type highly doped germanium (HD-Ge) layers ($N_{D,Ge} = 5\times10^{19}$ cm^{-3}), 100 nm in thickness, were deposited with antimony as the dopant at temperatures of 300 and 500 °C. Also deposited were intrinsic germanium (*i*Ge), 1 µm in thickness, also at temperatures of 300 and 500 °C. These were capped with a highly doped n-type Ge layer to improve contact ohmicity. 400 nm of Ni was sputtered onto the Ge surfaces and patterned using a lift-off process creating dots 200 µm. These were formed into mesa diode structures by etching the remaining Ge. Ni was also sputtered onto the back SiC surface to form a back contact.
The surface quality of the layers was assessed using x-ray diffraction (XRD) and atomic force microscopy (AFM). Crystalline cubic Ge and SiC peaks are evident within the theta-2theta scans of Figure 1. They all show the SiC peaks, however, the Ge peaks are more pronounced in the thicker *i*Ge layers compared to the HD-Ge layers, and, in the higher temperature layers compared to the lower temperature layers. This suggests that the lower temperature growths do not have enough energy to form in the Stranski-Krastanov regime of the higher temperature depositions, and end up forming a smooth, amorphous layer. Further evidence of this is in the AFM micrographs of Figure 2. The low temperature depositions show only polishing marks from the SiC beneath and have a surface roughness of 3-4nm, whereas the higher temperature layers show real evidence of island formation, especially in the 100nm thick HD-Ge layer. Clusters such as these occur when atoms deposited on a surface seek an atomic site that minimises the total energy of the system [4].

Current-Voltage results, shown in Figure 3, have yielded ideality factors for the *i*Ge diodes of $\eta = 1.1$, with the 500 °C diode allowing a reverse leakage current of only 9.1×10^{-9} Acm^{-2}. Such low ideality factors indicate that the current transport is dominated by thermionic emission and not recombination, thus proving the electrical quality of the Ge/SiC junctions. A built-in potential of 2 V, as extracted from the capacitance-voltage (C-V) measurements of Figure 4, is responsible for this low leakage current, though it also increases the resistance in the forward direction. The 500 °C HD-Ge diode displays the lowest forward resistance of the diodes and the lowest built-in potential of 1.5 V, most likely due to the thin Ge layer, its polycrystalline nature and its high doping. However it produces an ideality factor of η = 2.2, most likely due to patch contacts, where the Ge islanding allows both Ge and SiC to contact the nickel contact. All the diodes begin to turn on very early at approximately 0.3 V.

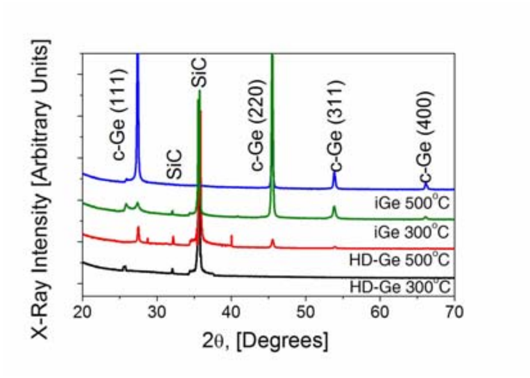

Fig 1: XRD θ-2θ scans of the MBE Ge layers deposited on 4H-SiC

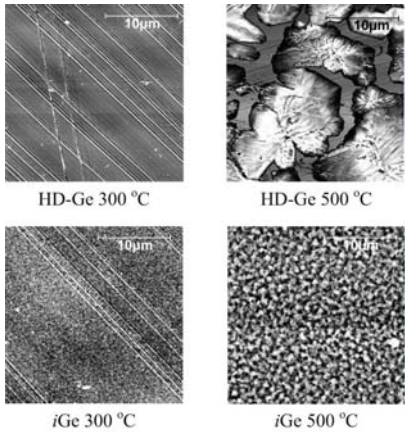

Fig 2: 25µm square AFM micrographs of the MBE Ge/SiC layers

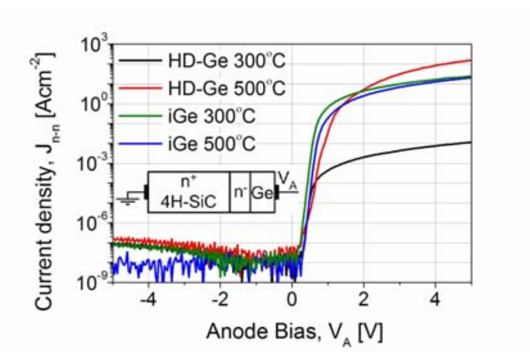

Fig 3: Semi-log I-V characteristics of the MBE Ge/SiC layers

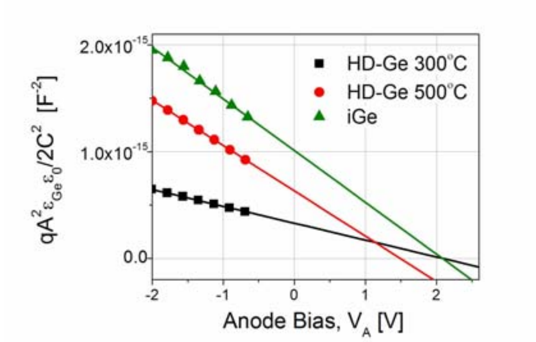

Fig 4: C-V characteristics of the MBE Ge/SiC layers

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Recent progress in diamond electronics

D.Doneddu [1,*], O.J.Guy [2], A.Castaing [2], M.Lodzinski [2]
[1] *Global Academy, University of Wales, Kings Road, Swansea SA1 8PH, UK*
[2] *School of Engineering, Swansea University, Singleton Park, Swansea SA2 8PP, UK*
[*] Corresponding author: d.doneddu@wales.ac.uk

Diamond is widely regarded as a promising material for use in electronics devices. Its superior performances in terms of mechanical, electrical, thermal and chemical properties make it the best candidate for high-frequency, high power devices, for use in a variety of environments, especially under extreme conditions [1]. Its figures of merit for power performance far outreach any other semiconducting material (see Table 1). Its biocompatibility is also paving the way for use of diamond devices in medical and biological applications. Single-crystal CVD diamond is, amongst the various forms of diamond, the type that in theory offers the highest performances [2]. Other types of synthetic diamond have recently been investigated which offer more processing flexibility, such as ultra-nanocrystalline diamond (UNCD) and nanocrystalline diamonds [3, 4].
Several recent advances on diamond power and high frequency devices have been reported such as high-temperature IGBTs [5], m-i-p diodes [6], and high frequency MESFETs [7-10] and diamond waveguides and detectors [11].
Diamond would be of particular advantages for combined high-temperature, high voltage and/or high frequency applications.
In this paper, an overview of recent advances in diamond electronics technology is presented.
Technology has currently exploited the limits of Silicon as a semiconductor material for power electronics devices. Requirements for ever higher voltage and current handling capabilities have paved the way for researching more exotic materials which offer superior power performances.
Diamond Schottky diodes, to be used as power devices, and more recently Schottky Barrier Photodiodes, or SPDs as Deep Ultra Violet (DUV) photodetectors [11]; diamond IGBTs [5] have also recently been proposed to address issues arising from operation under extreme conditions, such as within Jet Engines under development with the aim of achieving More Electronic Aircraft (MEA).
Another developing field is that of diamond as substrate for bio-sensors and bio-chips, given the supposedly higher biocompatibility and the inertness of diamond [12].
On the high-frequency side, recent developments on integrating optical waveguides on Silicon are currently extending the limits of this material for telecommunications, however, the need for stand alone high frequency devices means that other materials, such as diamond and also diamond coatings are being also exploited as they offer higher frequency operation. Diamond MISFETs and MESFETs have therefore been researched, and have been recently gaining more consideration [7-10].
Although research has reached major breakthroughs with the development of high quality single crystal CVD Diamond [2], its availability is still limited due to small quantities and very small wafer sizes thus making it not yet practical for commercial use. Concurrently, new developments on alternative diamond material technologies such as Ultra-Nano-Crystalline Diamond (UNCD) and Nano-Crystalline Diamond are experiencing a growing interest among the scientific and industrial community, due to the relative ease of producing substrates of suitable quality.
Research is also still being carried out on developing devices on thin film crystalline diamond for use as detectors and protein sensors [13].

	Si	4H-SiC	GaN	Natural Diamond	CVD Diamond	Potential device application benefit
Bandgap (eV)	1.1	3.2	3.44	5.47	5.47	High Temperature
Breakdown Field ($MVcm^{-1}$)	0.3	3	5	10	10	High Voltage
Electron Sat. Velocity ($x10^7$ cms^{-1})	0.86	3	2.5	2	2	High Frequency
Hole Sat Velocity ($x10^7$ cms^{-1})	n/a	n/a	n/a	0.8	0.8	
Electron Mobility ($cm^2V^{-1}s^{-1}$)	1450	900	440	200-2800	4500	
Hole mobility ($cm^2V^{-1}s^{-1}$)	480	120	200	1800-2100	3800	
Thermal Conductivity ($Wcm^{-1}K^{-1}$)	1.5	5	1.3	22	24	High Power
Johnson's FOM	1	410	280	8200	8200	Power-frequency product
Keyes' FOM	1	5.1	1.8	32	32	Transistor behaviour thermal limit
Baliga's FOM	1	290	910	882	17200	Unipolar HF device performance

Table 1 Intrinsic Material Properties and Figures of Merit (FOMs), at room temperature for Si, 4H-SiC, GaN, Diamond, and potential benefits

SBDs.

The relatively simple structure of Schottky-Barrier Diodes, coupled with the intrinsic lower barrier height characteristic of Schottky contacts, has traditionally made them the first candidate to provide a suitable replacement for traditional Silicon diodes. Recent work in UK has shown promising results, with devices reported to be able to withstand breakdown voltages of few kilovolts, within very thin drift layers (less than 25µm). As we can see from [14], temperature and drift doping concentration have major influences on the diamond SBDs behavior when forward biased, in particular, for medium doped drift layers, the higher activation energies are compensated during operation at higher temperatures, giving increase in forward conduction, despite the reduction in mobility. Research on termination techniques and materials, and modelling thereof, has also been recently reported, with a comparison between SiO_2, and Al_2O_3 [15] and different termination techniques, such as ramp oxides, using again high-*k* dielectrics [16].

Work focussing on contact quality aimed at producing ohmic and Schottky contacts has been published by this group [17-19]. Breakdown voltages in the order of 1kV without edge termination were then reported [18]. Experiments showed that breakdown was for some diodes originating at the periphery of the SBD due to leak currents and proceed on a lateral direction. This is in agreement also with [20]**.** Diamond SBDs have also recently been reported to exceed 1.6kV without edge termination, due to novel Pseudo-Vertical structures, and improved metal contacts, with the use of molybdenum [21]. However, the highest breakdown voltage recorded to date for an SBD is still 6kV, for devices obtained by J.E. Butler et al. in 2002 [22].

Parallel to single-crystal diamond, research has been recently focussing on UNCD and NCD diamond and p-type single-crystal - n-type UNCD heterostructures. Devices have been reported, with stable operation up to temperatures in excess of 1000 °C [3], and recent study on the material [4] are towards understanding the properties of UNCD upon temperature variations.

IGBTs

Recent studies in the UK aim at producing Diamond Insulated-Gate Bipolar Transistor (IGBT) for use at high temperature (in the range of 400 °C), for aerospace applications. At such high temperatures, the activation energy of n-type dopants in diamond has been show to drop dramatically, all impurities becoming ionized, and therefore carrier density should increase significantly. However, to date, only simulation results have been reported [5]

FETs

Diamond MESFETs have been proposed in recent years [7, 8, 9] on polycrystalline diamond, and are being developed by UK companies using single-crystal CVD diamond [10, 23].

Due to the lack of a shallow n-type dopant, and the high ionisation energy of B-doped diamond, influences the design and challenges traditional Silicon-based designs. Attractive designs include p-i-p MISFET, obtained through etching a trench through the doped conducting layer and by depositing gate dielectric and metal into the trench, exploiting the space-charge concepts outlined by Ikeda et al. [24]. This type of design however suffers from sensitivity to gate parameters. Another promising technique to circumvent the incomplete ionisation of dopants at room temperature and also investigated for diamond diodes, is the delta-doped structure (Fig. 1), for use for example in MISFETs [25]. Diamond FETs are currently subject of careful consideration for commercial purposes, and will probably be the first devices to enter the electronics market in the near future.

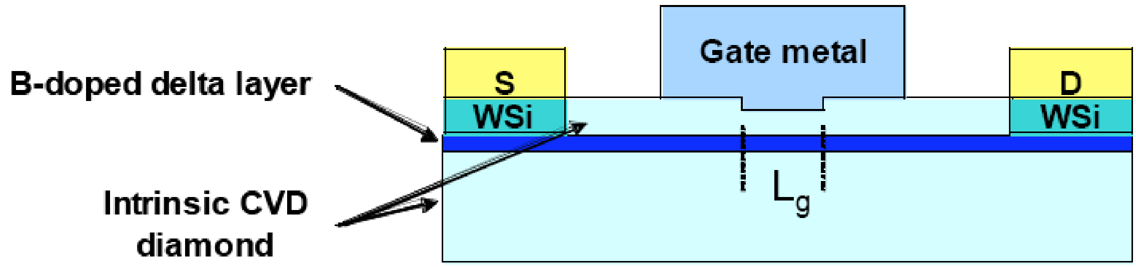

Fig. 1: Delta-doped diamond MESFET

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Metal contacts to boron-doped diamond

M. Lodzinski[1*], O.J. Guy[1], A. Castaing[1], S. Batcup[1], S. Wilks[1], D. Doneddu[2] and P. Igic[1]
R. Balmer[3], C. Wort[3], R. Lang[3]
[1]*School of Engineering, University of Wales Swansea, Singleton Park, Swansea SA2 8PP, UK*
[2]*Global Academy, University of Wales, Kings Road, Swansea SA1 8PH United Kingdom*
[3]*Diamond Microwave Devices Ltd, 103 Clarendon Road, Leeds, Yorkshire, LS2 9DF*
[*] Corresponding author: M.LODZINSKI.443395@swansea.ac.uk

Diamond's electronic and physical properties make it perhaps the most exciting material for high-power, high-frequency electronics. However, processing technology for diamond is still relatively rudimentary, and the problem of metal contacts to diamond has not yet been solved. This paper describes the fabrication of Ni and Ti contacts to single crystal, boron-doped diamond. The electrical performance of metal-diamond contacts has been investigated using current-voltage I(V) characterization of circular transmission line model (CTLM) test structures. X-ray photoelectron spectroscopy (XPS) analysis of Ti/diamond contacts has been performed and is correlated with CTLM results. Post deposition annealing of metal-diamond contacts has a dramatic influence on contact resistivity, with lower resistances observed after annealing at 900ºC. Specific contact resistances as low as 9×10^{-5} Ω.cm^2 have been obtained. The effect of doping (via epitaxial growth and boron implantation) on metal-diamond contacts is also reported.

Among the wide band-gap semiconductors, diamond is potentially the ultimate material for high-power, high-frequency electronics. It exhibits one of the highest band-gaps, breakdown field strengths, carrier mobilities and thermal conductivities of any semiconductor material. These extreme properties have driven the development of single-crystal semiconductor quality diamond, for devices with applications in the RF and power electronics industries [1, 2, 3].

Several authors have reported high-voltage Schottky diodes and high-frequency surface devices [4]. All these devices require metal-semiconductor contacts to diamond. Though there are numerous reports of rectifying Schottky contacts and low resistance Ohmic contacts to diamond, currently there is no standardised fabrication process for either type of contact [5].

There are several variables which affect the performance of metal-diamond contacts including: the contact metal; the contact metal thickness; contact annealing conditions; diamond surface termination and surface preparation; and the semiconductor doping [6].

Another important factor, when considering metal-diamond contacts, is the diamond surface which can have several different terminations (oxygen, hydrogen or carbon terminated). Properties of metals deposited on the diamond surface are highly dependent on the the different electron affinities of each surface termination – which influences the Schottky barrier height. Surface pre-treatment and growth techniques are thus critical factors determining the properties of metal-diamond contacts. By modifying the diamond surface chemistry, the contact behavior (Ohmic or Schottky) can be controlled.

The semiconductor doping N also influences the type of contact formed, as the depletion layer width w of a metal–semiconductor contact is proportional to $N^{-½}$. As w decreases with increasing N thus, the probability of tunnelling through the Schottky barrier increases, creating a lower resistance contact. Contacting to a highly doped diamond layer is therefore critical in forming a good Ohmic contact.

Ni and Ti contacts have been fabricated on both oxygen and hydrogen terminated surfaces. Electrical characterisation of CTLM patterns, based on the method developed by Marlow and Das, have been used to extract specific contact resistances. Contacts to hydrogen-terminated diamond showed lower contact resistances than those on oxygen-terminated diamond. All the samples were a subject to further annealing steps in order to create more intimate contacts and

improve the specific contact resistance. The optimum anneal temperature was around 900ºC after which specific contact resistances as low as 9 x 10^{-5} $\Omega.cm^2$ were obtained. XPS analysis of Ti/diamond contacts showed titanium carbide formation resulting after deposition of Ti on diamond. The amount of carbide formed increased after post metal deposition annealing of the contacts (Fig. 1). The effect of doping on specific contact resistances has also been investigated. Highly boron-doped diamond can be produced via epitaxial growth or by ion-implantation of low-doped diamond. Highly boron-doped delta layers (doped layers of less than 20 nm in thickness) have been compared to boron-implanted diamond samples, implanted with different boron doses and energies. The highest concentration boron implant (10^{20} cm^{-3}) produced the lowest contact resistances after annealing at 900ºC (Fig 2). These contact resistances were comparable to contacts formed on epitaxial boron doped diamond.
Boron- implanted samples showed similar behavior to epitaxial layers of boron doped diamond. In all cases the specific contact resistance improved with annealing up to 900ºC. At this temperature there is significant TiC formation, shown in XPS analysis, implying that TiC formation assists the formation of low resistance Ohmic contacts.

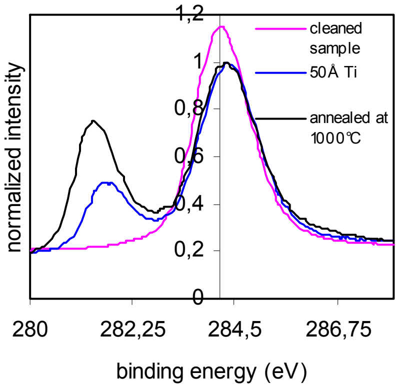

Fig. 1: C 1s peak of the XPS sample showing evolution of TiC after deposition of 50 A Ti and subsequent annealing at 1000ºC.

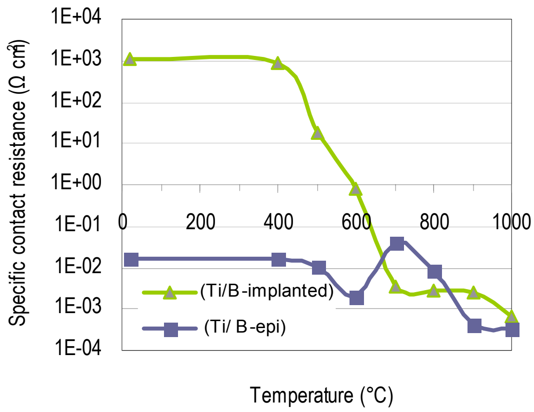

Fig. 2: Specific contact resistances of Ti contacts to boron-implanted and epitaxial boron-doped diamond as a function of PDA temperature.

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GaN/AlGaN HEMTs for RF Applications

E. Limiti*, W. Ciccognani, M. Ferrari
Dipartimento di Ingegneria Elettronica, Università di Roma "Tor Vergata",
Via del Politecnico 1, 00133 Roma, Italy
* Corresponding author: limiti@ing.uniroma2.it

GaN HEMT devices have gained a large popularity and many research efforts have been devoted to exploit their power performance at microwave and even millimeter wave frequencies. Given their inherently higher power density, GaN HEMTs are the key candidates to replace GaAs-based power amplifiers wherever a considerable output power is required to the transmit subsystem. Nevertheless, a series of RF and microwave applications require the development and availability of different functionalities, preferably adopting the same technology and eventually integrated with the high power amplification stage. This is the reason for the increasing interest in GaN HEMTs as basic active devices implementing, among the others, low noise (LNA), switching (SPDT or others) and mixing functions. As an example, in Fig. 1 the schematic representation of a single polarization transmit-receive (T/R) module is depicted, in which the presence of single-pole/double-through switches, as well as LNA modules is indicated together with the HPA.

Towards such further development, two major concerns arise: on one hand the beneficial and peculiar properties of GaN-based devices should be exploited, while on the other, if such properties are not directly related with the specific function, the functionality has to be implemented making use of the high power technology, not resurrecting to different epi or substrates, thus easing the subsequent integration.

As an example of the abovementioned problems, two recent developments will be presented in the following, regarding a broadband low noise amplifier and a high power switch, both of the narrowband and broadband type.

Regarding the LNA, the exploitation of the material system properties actually implies a much higher device robustness to incoming signals, thus leading to the elimination, in the T/R module scheme, of limiter often used to this goal (see figure 1), with beneficial effects in the overall system noise figure: in fact, even if GaN HEMTs exhibit comparable noise performance if compared to traditional GaAs PHEMTs, system simplification results in a remarkable increase in module sensitivity. As an example of this concept, in Fig. 2 the microphotograph of a three stage broadband amplifier chip is depicted. The adopted monolithic technology is a microstrip 0.25 um GaN HEMT by Selex SI, integrating also passive components (MIM capacitors, spiral inductors, Vias ...). The amplifier is composed by the cascade of three distributed amplifiers, composed each by two active devices. Target operating bandwidth is 2-18 GHz, and the topological design choices actually reflect the need to sustain high frequency gain of the amplifier. Measured performance is reported in Fig. 3, where small signal gain and noise figure are reported, while in Fig. 4 power performance is depicted, stressing the high power handling and ruggedness of the realized amplifier.

As a further example of GaN HEMT functionality, Fig. 5 depicts the microphotograph of a broadband single pole duble through switch, designed to operate from 2 to 18 GHz. Also in this case the adopted technology is a microstrip 0.25 um GaN HEMT one, by Selex SI. Measured performance is reported in Fig. 6 regarding the switch insertion loss as a function of frequency and in Fig. 7 regarding the power handling properties. As it is possible to note, power handling is well over the 40 dBm limit, thus encouraging the adoption of a switching function replacement instead of the isolator/circulator arrangement (see Fig.1).

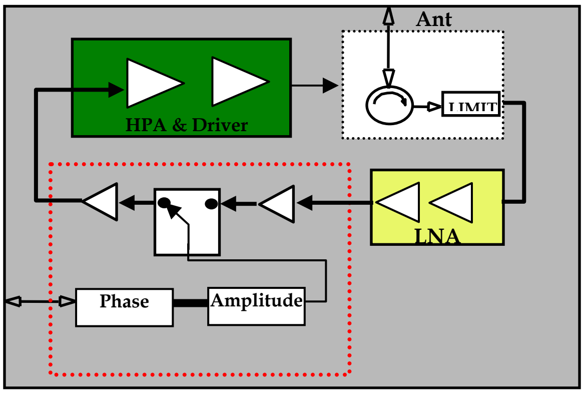

Fig. 1: Typical T/R module schematic (separate architecture)

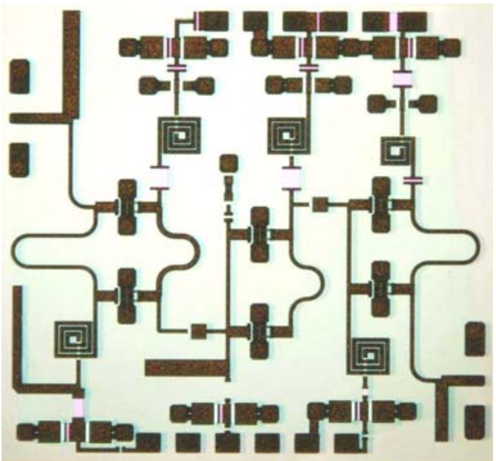

Fig. 2: Broadband LNA microphotograph

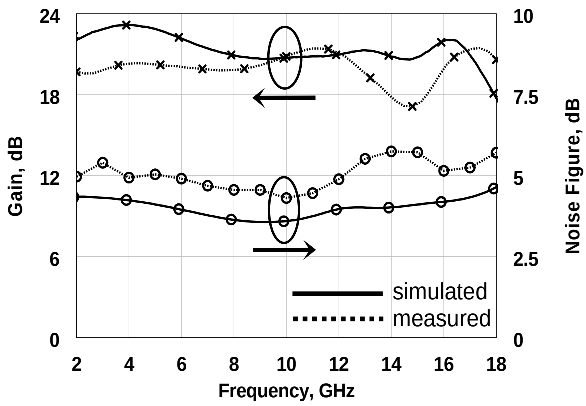

Fig. 3: Broadband LNA simulated and measured performance, small-signal gain and noise figure

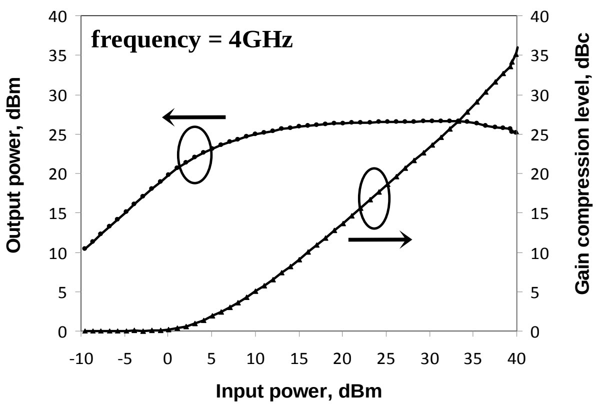

Fig. 4: Broadband LNA measured performance, output power and compression

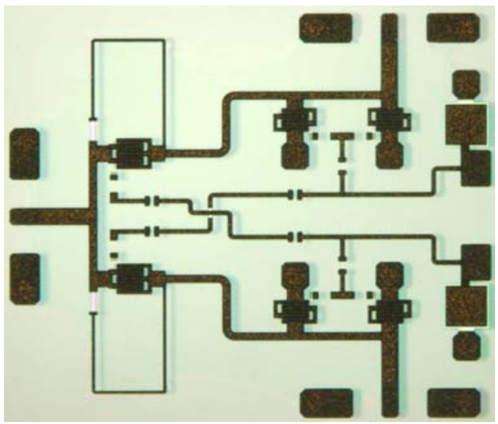

Fig. 5: Broadband Switch microphotograph

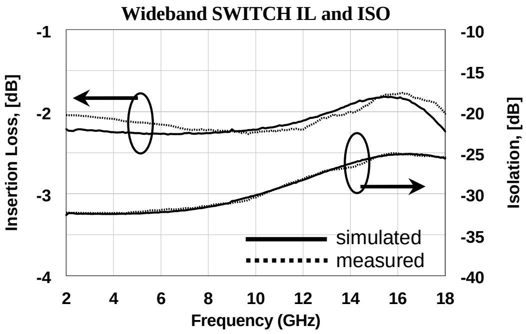

Fig. 6: Broadband Switch simulated and measured performance: insertion loss and isolation

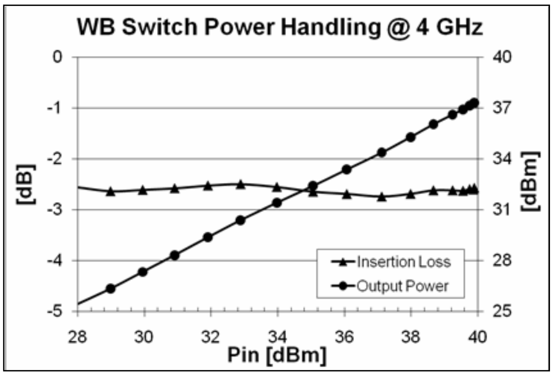

Fig. 7: Broadband Switch measured performance: output power and insertion loss

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Design, process, and performance of all-epitaxial double-gate trench SiC JFETs

Rajesh Kumar Malhan[1*], Yuuichi Takeuchi[1], Naohiro Sugiyama, Adolf Schöner [2]
[1] *DENSO CORPORATION, Research Laboratories, Nisshin, Aichi 470-0111, Japan*
[2] *ACREO AB, Electrum 236, Isafjordsgatan 22, SE-164 40 Kista, Sweden*
[*] Corresponding author: rajesh_k_malhan@denso.co.jp

Environmental concerns due to global warming are boosting the development of silicon carbide (SiC) power devices for industrial and automotive power switching applications. SiC power devices can potentially eliminate the costly cooling arrangements present in today's Si power electronics and can facilitate high power density systems due to low losses and high operation temperature capabilities [1]. The voltage-controlled junction field effect transistors (JFETs) are excellent candidates to fully exploite the SiC potential since they are free of gate oxide high temperature reliability and forward bias voltage degradation issues. SiC JFETs take advantage of the wide band-gap of the 4H-SiC material (Eg= 3.2 eV) and are quickly proving to be the most robust devices for high temperature power applications in excess of 200 °C.

This paper present an innovative all-epitaxial double-gate trench JFET (DGTJFET) structure, which seeks to overcome the power density limitations of conventioanl normally-*on* or -*off* JFETs. The DGTJFET design combines the advantages of lateral and buried gate JFET concepts. The lateral JFET advantage is the epitaxial definition of the channel width and the buried gate JFET advantage is the small cell size. In the DGTJFET process the epitaxial embedded growth in trenches facilitates the small cell pitch and the vertical direction of the channel. New migration enhanced embedded epitaxy ME^3 and planarization processes were developed to realize DGTJFETs for high-density power integration. The combination of design [2] and developed processes [3] enables a vertical channel with sub-micron width without sub-micron photolithography. The highly doped vertical channel of the DGTJFET defined by the ME^3 growth process makes it possible to accurately control the sub-micron channel dimensions to realize low specific on-state resistance R_{ON}, high saturation current and fast switching capabilities. The requirement of maximizing the channel doping for the fast switching speed of the normally-*off* JFET coincides with the requirements for the improved high temperature operation [4]. The anisotropic doping nature of SiC is taken into account for the DGTJFET channel design. A detailed numerical simulation analysis and successful applications of developed process technologies of all-epitaxial normally-*on* or -*off* 4H-SiC DGTJFETs will be discussed in detail at the workshop.

Fabricated 5.5 μm cell pitch DGTJFETs demonstrate the saturation current density J_{DS} capability of more than 1000 A/cm^2, inline with simulation results. R_{ON} of 5.5μm cell pitch N-*off* 4H-SiC DGTJFET is found to be 2.6 mΩcm^2 at gate voltage V_G of 2.5 V and drain voltage V_{DS} of 1.0 V. Normally-*on* DGTJFET device with an active area of 0.106 cm^2 and 9.5 μm cell pitch outputs 100 A at V_G of 2.5 V and V_{DS} of 5.5 V. The roon temperature R_{ON} of the normally-*on* DGTJFET is about 4.8 mΩcm^2 at J_{DS} of 414 A/cm^2. We expect continuous JFET technological improvement for higher power and system level fail-safe operation demonstration with new control drive methodologies in the near future.

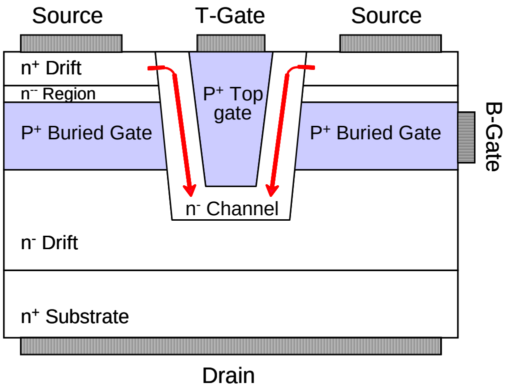
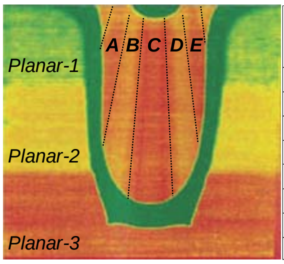


Fig. 1: Schematic drawing of all-epitaxial SiC double-gate trench JFET (DGTJFET).



	SSRM Signal [V]	Al Conc. [cm^{-3}]
Planar-1	1.05	$5.5x10^{16}$
-2	0.80	$1.7x10^{17}$
-3	0.29	$1.7x10^{18}$
Region-A	0.25	$1.9x10^{18}$
B	0.49	$6.5x10^{17}$
C	0.15	$3.0x10^{18}$
D	0.46	$7.5x10^{17}$
E	0.24	$2.0x10^{18}$

Fig. 2: 2D Al-dopant distributions in the embedded trench structure (SIMS and SSRM investigations).

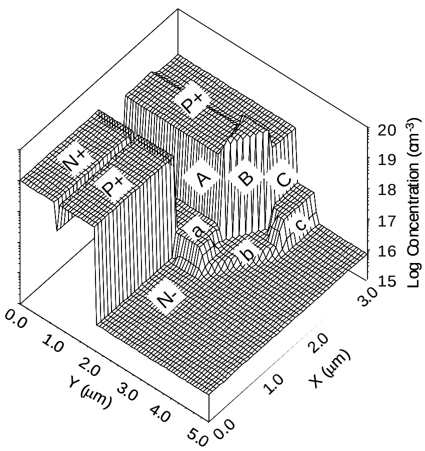


Fig. 3: N and Al dopant concentration 3D profiles of embedded trench structure on C-face SiC wafer.

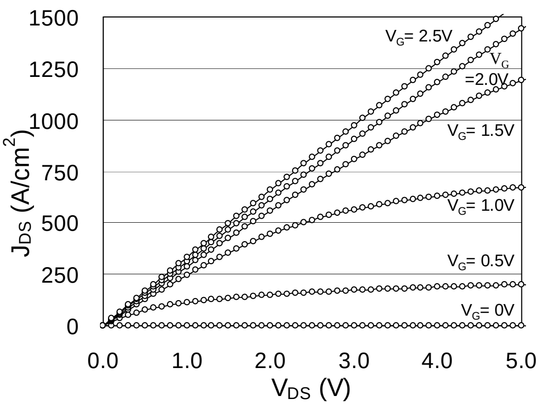


Fig. 4: Simulated output characteristic of DGTJFET with anisotropic conditions for a Si-face SiC wafer.

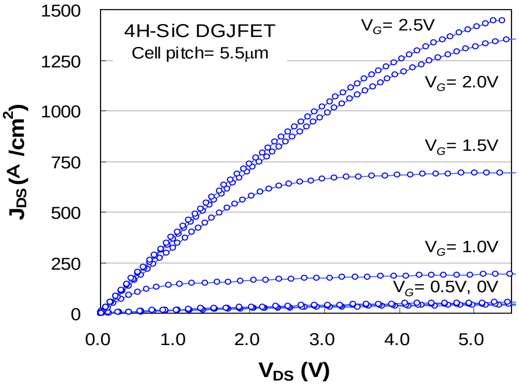


Fig. 5: Output characteristic of fabricated 5.5 μm cell pitch normally-on 4H-SiC DGTJFET.

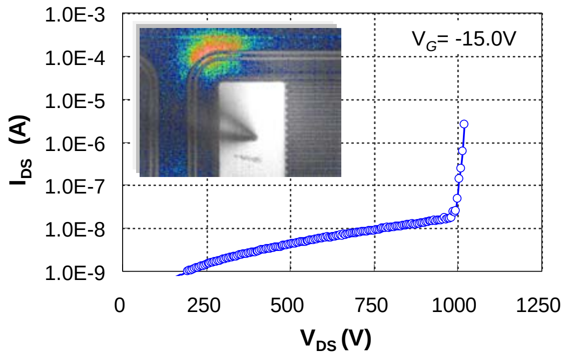


Fig. 6: Breakdown characteristics of normally-on 4H-SiC DGTJFET. Inset emission microscope image shows the breakdown location at the device termination edge.

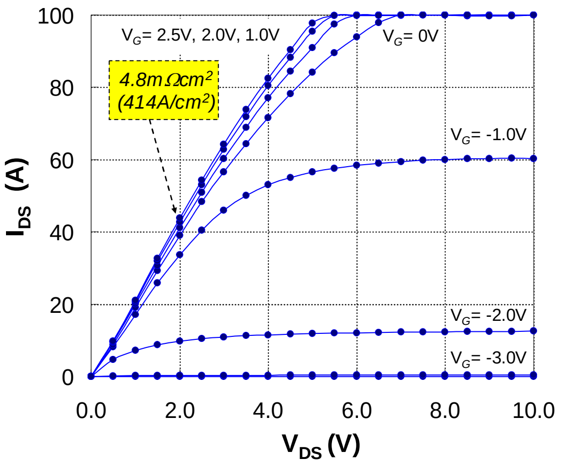


Fig. 7: Output characteristic of fabricated 9.5μm cell pitch normally-on 4H-SiC DGTJFET.

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Prospects and Challenges for GaN HFETs in Wireless Basestation Applications

Peter Asbeck *
University of California, San Diego, La Jolla, CA, USA 92093
* Corresponding author: asbeck@ece.ucsd.edu

Power amplifiers for wireless basestations must meet stringent requirements of linearity while amplifying large signals (peak power above 200W) with high peak-to-average ratio (above 7dB). Amplifier efficiency is a key consideration for commercial application. GaN devices are receiving considerable attention since they demonstrate better results than Si LDMOS competitors. In our work, the Envelope Tracking technique has been used together with adaptive digital predistortion to achieve power added efficiency above 50% using GaN on Si HFETs in WCDMA basestation amplifiers [1]. Figure 1 illustrates the ET system, in which the power supply voltage is dynamically changed in accordance with the signal envelope. Figure 2 illustrates measured efficiency of the RF stage vs output power at 2.14GHz as the envelope is varied with a WCDMA signal. For most envelope levels, the GaN device operates with efficiency above 75% (while the remaining inefficiency is due to the variable drain voltage supply) . The remarkably high HFET efficiency and its constancy over operating voltage, result from high drain voltage relative to knee voltage, and low output capacitance of the GaN devices. Impedance matching intermediate between Class E and Class F^{-1} is used (which changes as the drain voltage varies because of the voltage dependence of the output capacitance). Memory effects from the GaN HFETs are found to be negligible in the 10-100MHz range.

An important feature of the GaN HFETs is their ability to operate at high drain voltages, as a result of the high breakdown electric field of GaN. It has been widely noted that the I-V characteristics, particularly near the "knee" between dc and pulsed operation can change depending on the drain and gate bias. This "current slump" and the drain voltage dependence of Vt affect the RF output power vs drain bias of the devices. We have modeled the effect using physically-based simulations, and also with a compact model for circuit simulation [2]. Figure 3 illustrates measured pulsed Id-Vds characteristics under various quiescent biases (for a device with significant knee voltage walkout) and for comparison is shown the simulated characteristics. With the compact model, shown schematically in fig. 4, the experimental dependence of output power on drain bias for a representative PA with current slump is predicted, as shown in figure 5. The devices shown here have no field plates. Use of field plates diminishes, but does not eliminate, the effects.

For RF power as well as for lower frequency switching applications, the Baliga figure of merit, $\mu\varepsilon\ E_{bk}^3 \sim BV^2/R_{on}$ is an important figure of merit. GaN exhibits values 100x better than Si. Still, devices have been shown to operate successfully with voltages and resistances that are even better than this figure of merit [3]. With GaN HFETs there are intrinsic mechanisms that fulfill a function analogous to the resurf strategy well established in Si technology. A key consideration is the variation with time (and drain voltage) of the charge at the nitride surface. Figure 6 depicts the basic charge distributions in the HFET as a result of polarization effects and surface states. Figure 7 illustrates mechanism that produce changes in surface charge as a result of device bias conditions. The anomalously high breakdown in GaN HFETs results from the induction of negative charge at the nitride surface during high drain voltage operation. For future optimization of GaN HFETs, improved understanding and better control over these mechanisms is required.

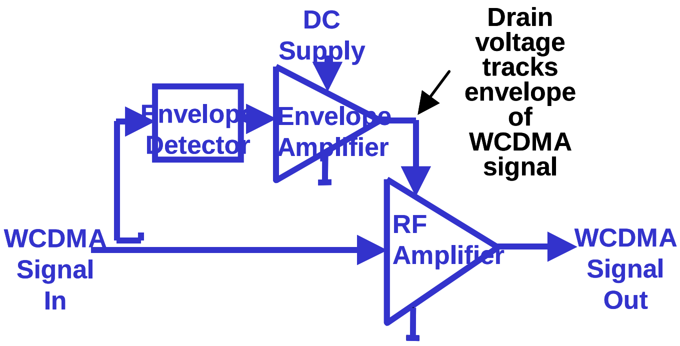

Fig.1: Schematic diagram of Envelope Tracking base station power amplifier.

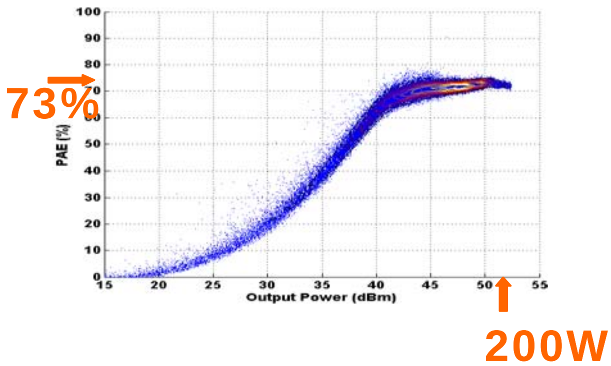

Fig.2: Instantaneous power-added efficiency vs output power for a GaN HFET measured during WCDMA operation in an ET amplifier.

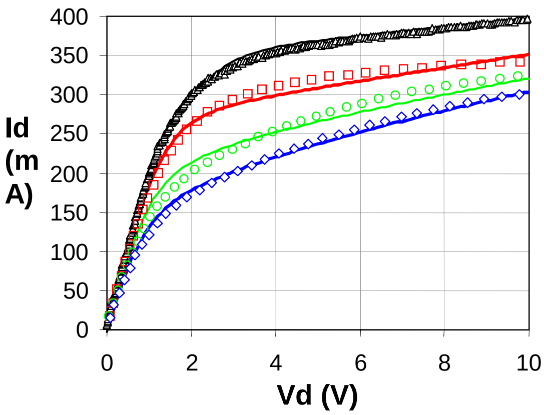

Fig.3: Measured Id-Vds characteristics for an AlGaN/GaN FET in pulsed operation, for various quiescent biases. The top curve corresponds to dc operation. Also shown are simulated curves from a physics-based model.

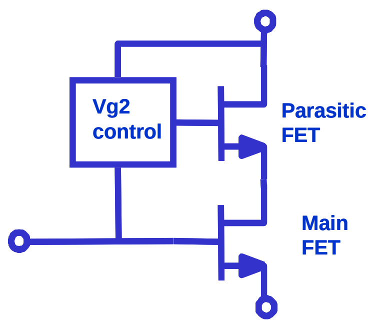

Fig. 4: Schematic diagram of virtual gate model of GaN HFET.

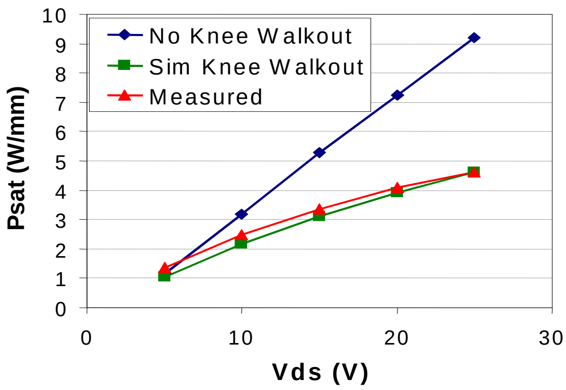

Fig.5: Experimental and simulated RF power vs drain supply voltage for GaN HFET (no field plate)

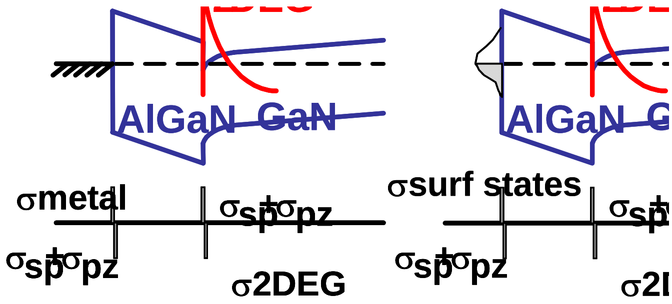

Fig. 6: Schematic diagram of charge balance associated with GaN HFET, under the gate and in the gate-drain gap.

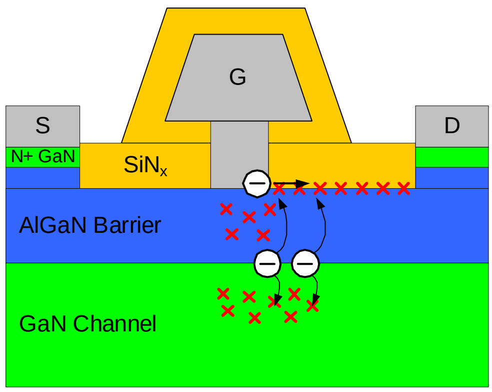

Fig.7: Illustration of various mechanisms for producing voltage-dependent charges adjacent to GaN HFET channel.

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Development of 100mm Semi-Insulating SiC for RF Devices

A. Souzis*, A. Gupta, I. Zwieback, T. Anderson
II-VI Incorporated, Wide Bandgap Materials Group, PO Box 840, Pine Brook, NJ 07058 USA
* Corresponding author: asouzis@ii-vi.com

II-VI has developed large-diameter SiC substrate manufacturing capabilities for both the GaN and SiC based semiconductor device markets. For the RF – GaN market, II-VI has applied its Advanced PVT (APVT) process for the growth of vanadium-compensated semi-insulating (SI) 6H SiC single crystals suitable for commercial manufacturing of high quality 100 mm diameter SiC substrates. Bulk crystal growth, wafer fabrication, polishing and surface preparation processes were developed, building upon our 3" manufacturing experience. Micropipe density in the 100 mm 6H SI substrates ranges from 1 to 6 cm^{-2} and total dislocation density between $2 \cdot 10^4$ and $4 \cdot 10^4$ cm^{-2}. X-ray rocking curves measured on 100 mm 6H wafers showed edge-to-edge lattice curvature ($\Delta\Omega$) between 0.1° and 0.3° with FWHM of the (0006) rocking curve between 30 and 75 arc-seconds.

In general, sublimation growth has been carried out in the temperature range between 2000°C and 2300°C, under a small pressure of inert gas. The specific growth conditions and sublimation geometry depended on the growth process objective, whether it was to increase the crystal diameter, generate high-quality seeds or to produce prime semi-insulating material for sale.

A key crystal growth achievement was development of a special growth technique for diameter expansion. This process resulted in large diameter wafers with high quality material in the expanded area. This technique was developed based on extensive finite element modeling, which helped to optimize thermal gradients in the growth crucible.

In the manufacturing process for semi-insulating crystals, vanadium is added to the growth charge to compensate for residual shallow donors (N) and acceptors (B). Vanadium compensation results in high and spatially uniform resistivity, on the order of 10^{10}-10^{11} Ohm-cm. In order to avoid yield losses due to non-uniform resistivity, a special doping technique was developed to deliver precise and steady flow of vanadium vapor to the growing crystal.

The grown boules are fabricated into wafers using multi-wire diamond saw technology. Slicing parameters for large-diameter SiC ingots were optimized to enable production of wafers with minimum warp and good flatness. Scale-up of our state-of-the-art 3" mechanical polishing and chemical-mechanical polishing (CMP) processes to 100 mm was relatively straightforward. The most significant task of the scale up was implementation of larger polishing tools.

Our standard evaluation of crystal quality includes imaging between crossed polarizing filters, determination of micropipe and dislocation densities and x-ray rocking curve topography. Cross-polarizer images of two 100 mm diameter, semi-insulating 6H-SiC substrates sliced from two different ingots are shown in Fig. 1. While both wafers are essentially free from major defects, the wafer in Fig. 1, left, shows the residual "mottled" contrast, which is due to the minor sub-grain mosaic structure in the right-hand part of the wafer. The image of the wafer in Fig. 2, right, which was sliced from another boule, shows practically no visible defects.

In order to determine micropipe and dislocation densities, the wafers were etched in molten KOH followed by mapping under a microscope using an automated image recognition system. Fig. 2, left, shows a micropipe density map measured on one of our latest 100 mm diameter 6H SI substrates. At present, the MPD values in our large-diameter 6H substrates are between 1 and 6 cm^{-2}. Fig. 2, right, shows a dislocation density map measured on another typical 100 mm 6H SI substrate; the total dislocation density in this wafer is about $2 \cdot 10^4$ cm^{-2}.

In general, the total dislocation density in our 100 mm 6H SI substrates is between $9 \cdot 10^3$ and $2 \cdot 10^4$ cm^{-2}.
X-ray quality of our 100 mm 6H SI substrates is evaluated using the technique of rocking curves. The measurements are performed on a high-resolution double-crystal diffractometer Philips 4001 using the symmetrical Bragg reflection (0006) with the following parameters: Ω mode, Cu Kα (λ=1.5406Å) line and beam size of 1 x 1 mm^2. Routine evaluation includes scanning the wafers from edge to edge along the <11-20> and <1-100> orthogonal diameters. Upon scanning, the data is recorded for the sample angle (Ω) and Full Width at Half Maximum (FWHM) of the reflection. The curvature of the lattice planes manifests as variation in Ω upon scanning; edge-to-edge variation (ΔΩ) is used as a measure of lattice curvature.
Fig. 3, left, shows x-ray Ω scans performed along <11-20> and <1-100> directions on a 100 mm wafer sliced from one of the typical 6H SI boule. The maximum value of ΔΩ for this boule is about 0.03°. The plot in Fig. 3, right, shows FWHM scans for the same wafer. One can see that for most of the points on the wafer surface the FWHM is below 50 arc-seconds.
Electrical resistivity of our 100 mm 6H SI substrates is measured and mapped at room temperature using COREMA, a non-contact capacitance-based instrument, which covers the resistivity range of 10^5 to 10^{12} Ohm-cm. A resistivity map of one of the 100 mm substrates sliced from 6H SI boule # EV-0009 is shown in Fig. 4. All wafers sliced from this boule are semi-insulating with the resistivity above 10^{10} Ohm-cm.
100mm diameter semi-insulating 6H SiC single crystals are grown at II-VI using the Advanced PVT growth process. The crystals are fabricated into high quality 100 mm 6H SI wafers with material properties and manufacturing yields similar to our 3” 6H SI material. These wafers are now routinely sold to commercial customers in the US, Japan and Europe for RF device development and commercial production.

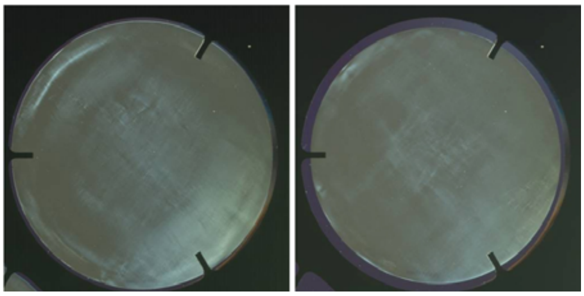

Fig. 1: Cross Polarizer images of two 100 mm wafers. Left – mottled contrast due to minor sub-grain. Right – no visible defect.

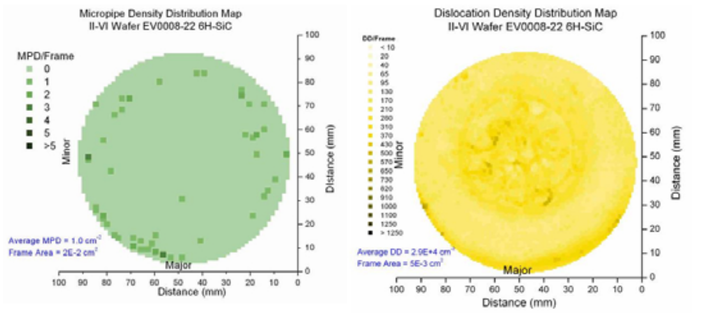

Fig. 2: - Left - Micropipe density map (MPD) of a 100 mm wafer. MPD = 1.0 cm^{-2} Right – Dislocation density (DD) map of 100 mm wafer. DD = 2.9E4 cm^{-2}.

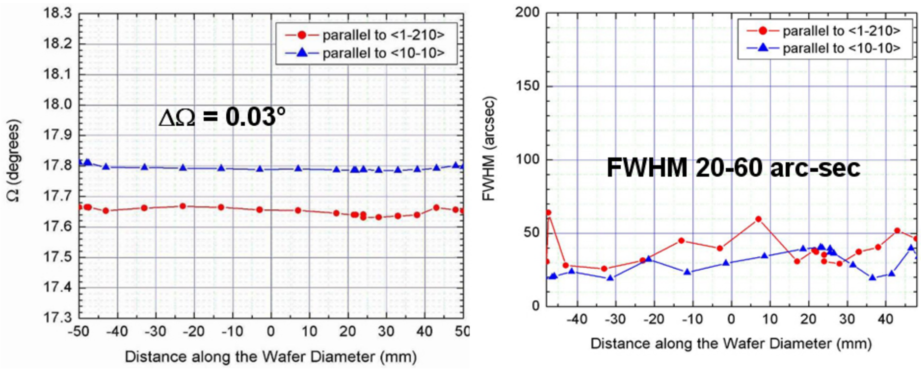

Fig. 3: X-ray evaluation of 100 mm 6H-SiC wafer Lattice Curvature ($\Delta\Omega$) = 0.03°. FWHM = 20-60 arc-second in 100 mm area.

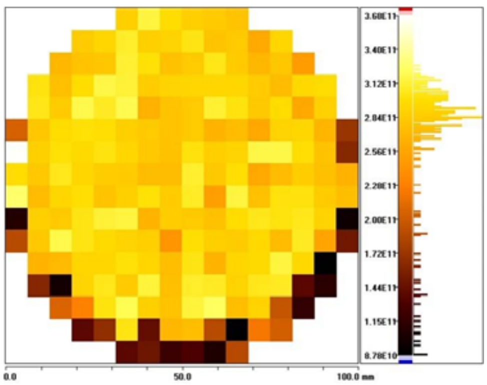

Fig. 4: Corema resistivity map of SI 100 mm wafer with a resistivity of 2.9E11 Ω-cm.

GaN/AlGaN HEMTs for RADAR applications

Claudio Lanzieri *
SELEX-SI s.p.A. - Engineering Division, Via Tiburtina Km 12.400 - 00131 Rome, Italy
* Corresponding author: clanzieri@selex-si.com

The increasing request of high power microwave components, has represented during the recent past as a driving force for the development of advanced technologies applied for monolithic microwave circuit (MMIC) manufacturing. This technology has found a specific employment inside the Tx/Rx modules for Radar, Avionics, Missile and Space applications.
At present the majority of solid-state microwave communication and radar electronics is based on GaAs semiconductor technology. Mature active device technologies (MESFET, PHEMT, MHEMT and HBT) are currently implemented to satisfy present market requirements.
Nevertheless GaN HEMTs have recently become a commercial reality and are an increasingly popular choice when power, linearity and robustness are required

The intrinsic advantage of GaN for high frequency and broadband amplifier applications can be related to the intrinsic basic material characteristic. GaN has an inherent breakdown field strength that is roughly 10 times that of silicon or GaAs. Thus, for similar device dimensions, a GaN device will have a drain-to-source breakdown 10 times that of a silicon or GaAs structure. This higher field strength can be used to increase power performance of unit device and/or to translate the required GaN transistor into a physically smaller active area which results in a significant reduction in terminal capacitive feedback increasing the intrinsic device bandwidth and frequency response. Furthermore thermal conductivity of GaN/SiC is approximately 10 times that of GaAs. These high thermal conductivities will translate into lower peak operating temperatures, increased RF output efficiency, and improved device reliability. In terms of device frequency response, the electron mobility and the saturated electron velocity for GaN is compatible to device amplifier well into X-Band with the possibility of adequate performance into low mmW frequencies.
These performances improvement cannot be made possible for any of the other present semiconductor technologies.
GaN technology has already shown their capability for very high power application (HPA) and for robust Low Noise Amplifiers (LNA) can be realised. In addition, for the reason that of the high power handling also switches can be designed and fabricated able to replace the current ferrite circulators in Transmit/Receive (TR) modules
For these reasons, SELEX-SI foundry is actively involved in an extensive research project to develop and consolidate a reliable processing for GaN MMIC's production. In the frame of national and European project very high performance GaN HEMT device have just developed optimizing material properties and Field Plate technology.
In this presentation "state of the art" prototype developed for S Band, X- Band and Wide Band application, utilising two different technology schemes. i.e 0.5 and a.25 µm gate length, will be reported.

Three-Terminal Breakdown Evaluation in GaN-HEMT Devices

Augusto Tazzoli*, Enrico Zanoni, Gaudenzio Meneghesso
DEI, University of Padova, Via Gradenigo 6/B, 35131, Padova, Italy
*Corresponding author: augusto.tazzoli@dei.unipd.it

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are becoming optimum candidates for the fabrication of new high-power and high-frequency devices demanded by future wired and wireless communication applications [1]. In this work we have carried out a complete electrical characterization in DC and pulsed regime of traditional and T-Gate GaN HEMTs, extending the device bias up to the breakdown value. Devices were characterized by a Width (W) from 80 um to 1.2 mm, and a L_G of 0.5 um. Tested HEMTs were grown over SiC, Sapphire, SiCopSiC (mono-crystalline SiC on poly-crystalline SiC), and SopSiC (mono-crystalline Si on poly-crystalline SiC) [2]. A schematic representation of studied devices is shown in Figure 1.

A complete DC electrical characterization has been carried out using a Hp 4142 parameter analyzer under dark-light condition. All tested HEMTs showed good current levels, but, as expected, self heating effect affected the devices. Trapping effects and current collapse phenomena, that typically could impact on the reliability of GaN-HEMT devices [3], have also been characterized by means of a home-made double-pulser setup (Diva like). Figure 2 reports the I–V output characteristics of a W = 100 um SopSiC device measured at two quiescent bias points ((V_{G_bl}, V_{D_bl}) = (0 V, 0 V), and (-6 V, 20 V)). From the measurements, it is possible to notice the absence of trapping phenomena and a negligible current collapse.

We have used a 100 ns Transmission Line Pulser (TLP-TDR) [4] in order to study the behavior of HEMTs at high voltage and high current regimes. TLP technique is a traditional way to evaluate the reliability of devices under ESD-like events, but it can be also used for the characterization under high voltage and / or high current pulses. The I-V output characteristics of a W = 1 mm, device with V_{DS} up to about 75 V are reported in Figure 3. The device is less affected by self-heating effect than previously reported DC measurements, as expected, it shows some short-channel effect, but, at V_{GS} near to the pinch-off voltage and V_{DS} higher than 30 V, I–V curves change their linear slope going to assume an exponential behavior.

The breakdown voltage dependence with the Gate bias was also investigated. Figure 4 shows the I-V Output characteristics measured at different Gate voltage of a SopSiC HEMT, up to the reaching of the breakdown point. It is interesting to note that the breakdown voltage in pulsed regime varies from about V_{DS} = 90 V in open-channel condition (V_{GS} = 0 V, +1 V), increasing up to 300 V near to the pinch-off voltage (V_{GS} = -5 V). This trend can suggest that power dissipation and/or current density is playing an important role in determining the breakdown voltage. A similar behavior was shown also by SiC-based HEMTs, as shown in Figure 5. Iso-power curves are also depicted on Figure 5, and it can be observed that the breakdown point is not only determined by power dissipation, neither driven only by the Gate-to-Drain electric field (a decreasing of the breakdown voltage should be observed at decreasing of the Gate voltage). That is confirmed by I-V Output curves shown in Figure 6, measured on another SiC-based HEMT. A combined mechanisms, involving power dissipation, current density, and electric field, could then be responsible of the observed results. It is also interesting to note that in all the tested devices hard-breakdown (catastrophic) behavior is observed, contrary to GaAs devices that typically present soft-breakdown curves, see [5].

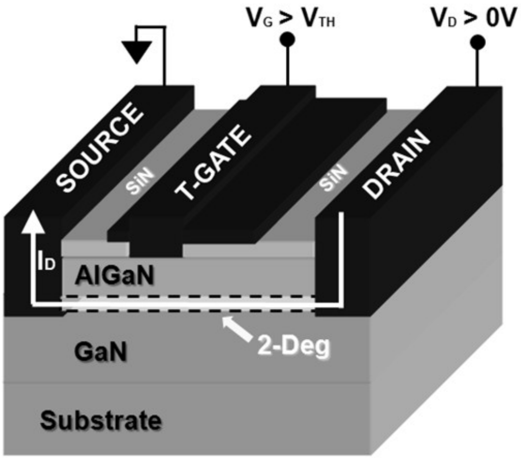

Fig. 1: Schematic structure of studied HEMTs. It is possible to note the field plate over the Gate contact (T-shape Gate). Artwork not in scale.

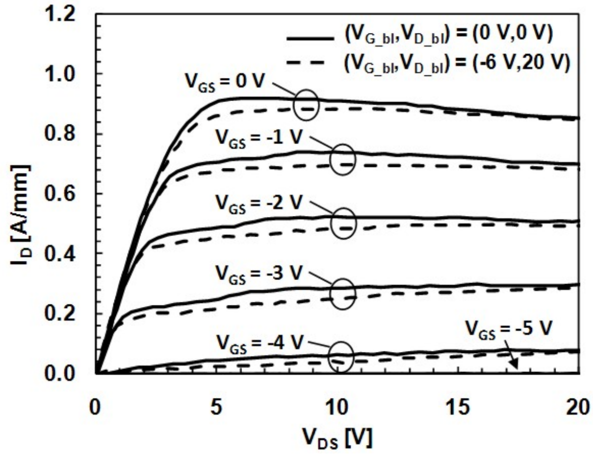

Fig. 2: DIVA-like measurements performed at two different quiescent bias points (W = 100μm, L_G=0.5μm, SopSiC). Pulse width/Period=1 μs/100 μs.

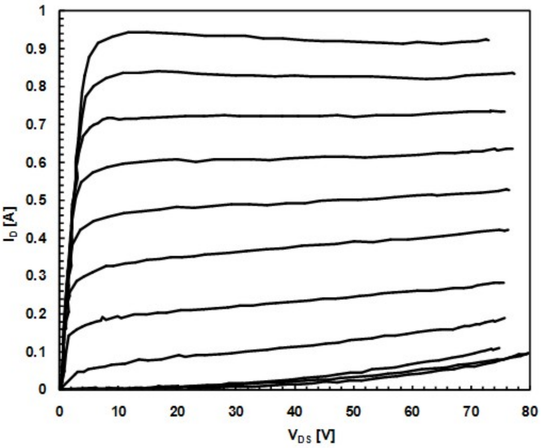

Fig. 3: I-V curves in 100 ns-TLP regime. Device width W = 1 mm, SiCopSiC. Gate bias: 0 V ≤ V_{GS} ≤ -5 V, step 0.5 V.

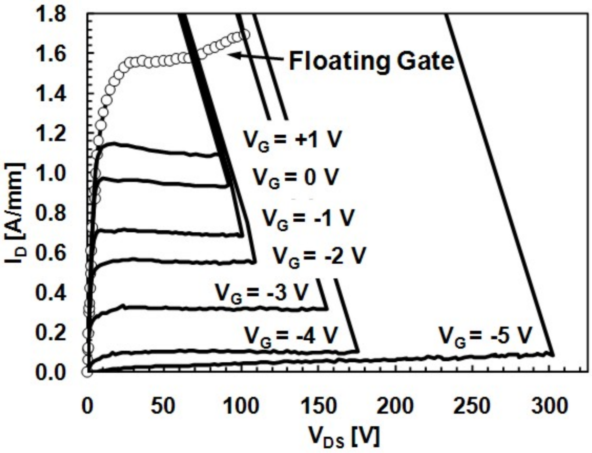

Fig. 4: I-V curves in 100 ns TLP regime to evaluate the breakdown points at different V_{GS}, and in floating gate condition (W = 800 μm, L_G = 0.5 μm, SopSiC).

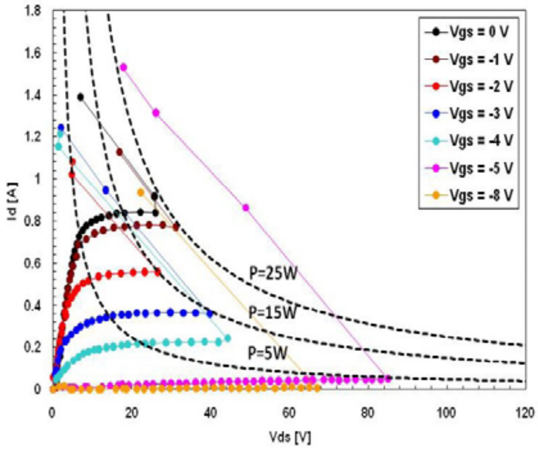

Fig. 5: I-V Ouput curves in 100 ns TLP regime to evaluate the breakdown points at different $V_{GS.}$ (W = 1000 μm, L_G = 0.5 μm, SiC).

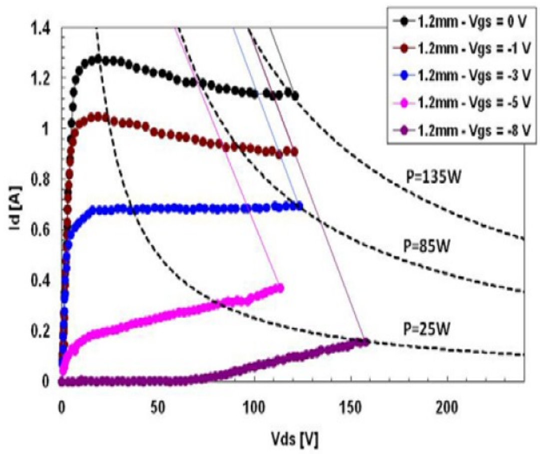

Fig. 6: I-V Output curves of SiC HEMT (W = 1200 μm) under 100 ns TLP regime. V_{GS} values are reported in the label.

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The influence of AlN/AlGaN/GaN transition layers on breakdown simulation of an AlGaN/GaN HEMT

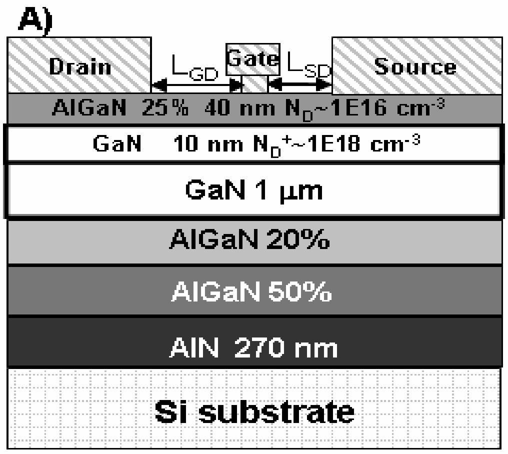
C. Miccoli[1,2 *], G. Abagnale[1], S. Reina[1], V. Puglisi[1], V. Cinnera Martino[1], S. Rinaudo[1]
[1] *ST Microelectronics, Stradale Primosole 50, 95121 Catania, Italy*
[2] *Dipartimento di Fisica e Astronomia, Università di Catania, Via S. Sofia 64, Catania, Italy*
[*] Corresponding author: cristina.miccoli@st.com

AlGaN/GaN high electron mobility transistors (HEMTs) exhibit electrical characteristics suitable for high power, high-frequency applications [1-4]. However, thick GaN layers useful for the production of RF/high power devices are limited by the mismatch, in lattice parameters and coefficients of thermal expansion, between gallium nitride and substrates used in GaN heteroepitaxy. The residual stresses caused by these mismatches are accommodated by the formation of misfit and threading dislocations ($10^7 \div 10^9$ cm^{-2}), which impact on the substrate quality and device characteristics.
The use of alternative substrates requires the inclusion of elaborated buffers. Actually, a reduction/elimination of tensile stress and dislocation density is obtained thanks to GaN or AlN interlayer, even if it depends on the growth conditions [5-6]. For these reasons, it is important to investigate the role of these layers with reference to device performance.
The study and analysis about the influence of AlN/AlGaN/GaN interlayers on HEMT electrical characteristics is the main subject of this contribution. Especially, thanks to device simulations, it is possible to optimize the structure layers in order to achieve the highest breakdown voltage.
The $Al_{0.25}Ga_{0.75}N$/GaN HEMT analyzed in this work is reported in the scheme (Fig. 1). At a first step a simple buffer layer is considered (see Fig. 1A) to calibrate simulation parameters thanks to experimental data. Then, device simulations are performed for more complex transitions layer structures (see Fig. 1B) with AlN, necessary to avoid cracks on GaN heteroepitaxial layers when the thickness of them is increased.
The two-dimensional device simulator used in this work was SILVACO Atlas [7]. Poisson equation and continuity equations for electrons and holes are solved, and drift-diffusion model is used to solve transport equations. The polarization field, due to spontaneous polarization and piezoelectric effect, is modelled in the usual way by specifying fixed sheet charges density (σ_{POL}) at the AlGaN surface and at the AlGaN/GaN interface. Experimental DC characteristics were available for AlGaN/GaN HEMT (Fig. 1), so it was possible to calibrate σ_{POL} as a fitting parameter. Also Selberherr's impact ionization model for GaN-compounds has been considered [8]. GaN breakdown electric field (Ec) is 3.41 MV/cm, while Ec is assumed equal to 1.1 MV/cm for AlN, as reported in literature [9,10].
The simulation is set in order to perform the drain–current injection technique, which enables easy measurement of off-state breakdown voltage in unstable and fragile devices, such as AlGaN/GaN HEMTs. The method is reported in [11] and simulation results show the same trend of curves in [11].
The aim of this analysis is to understand the roles of GaN thickness and of the AlN layer on HEMT breakdown. By structure in Figure 1, it is simple to notice that there are two layers of GaN: the first layer (T_1) is 1.6 μm thick, the second one (T_2) is 0.5 μm. A study of breakdown voltage is done varying T_1 and T_2; all considered cases are summarized in TABLE 1. It is easy to notice that the AlN/AlGaN/GaN transition layer play a key role in HEMT breakdown. A vertical cut-line under the drain contact shows that the AlN layer has an electric field peak value near the AlN E_c, and it exceeds that value just after the breakdown. So, that physical phenomenon competes with the breakdown of active layer, such as AlGaN/GaN, and probably it could have a deep influence on device performance. Those considerations can be applied to all cases considered.

In conclusion, the aluminium nitride layers are useful for the reduction of dislocation density, but simulation results underline that AlN could be crucial for HEMT breakdown.

Tab. 1: Scheme of structures simulated with different GaN thickness.

NAME	T_1 (μm)	T_2 (μm)	BV_{DS} (V)	BV_{DG} (V)
T1_6	1.6	0.5	221	312
T0_6	0.6	1.5	215	283
T1	1.0	1.1	208	286
T1-0_5	1.0	0.5	196	262



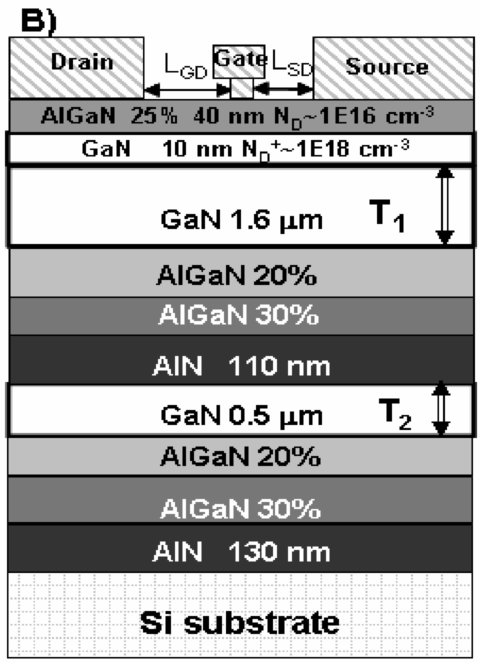


Fig.1: AlGaN/GaN HEMTs analyzed in this study. A) Structure realized and useful for the simulator validation. B) Complex buffer layer reproduced by simulations.

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Participants List

Name	Affiliation	e-mail
Abagnale Giovanni	ST Microelectronics - Catania ITALY	giovanni.abagnale@st.com
Abbondanza Giuseppe	LPE-ETC - Catania ITALY	g.abbondanza@etc-epi.com
Alquier Daniel	Université François Rabelais - Tours FRANCE	daniel.alquier@univ-tours.fr
Anzalone Ruggero	CNR-IMM - Catania ITALY	ruggero.anzalone@imm.cnr.it
Arrabito Giuseppe	Scuola Superiore – University of Catania ITALY	giarrabito@unict.it
As Donat Josef	University of Paderborn GERMANY	d.as@uni-paderborn.de
Asbeck Peter	University of California, San Diego USA	asbeck@ece.ucsd.edu
Bakowski Mietek	ACREO AB - Kista SWEDEN	mietek.bakowski@acreo.se
Bano Edwige	INP - Minatec - Grenoble FRANCE	bano@minatec.inpg.fr
Baratta Giuseppe	INAF - Astrophysical Observatory Catania ITALY	gbaratta@oact.inaf.it
Berthou Maxime	CSIC-CNM - Barcelona SPAIN	maxime.berthou@imb-cnm.csic.es
Beshkova Milena	University of Linköping SWEDEN	milbe@ifm.liu.se
Calcagno Lucia	University of Catania ITALY	lucia.calcagno@ct.infn.it
Camara Nicolas	CSIC-CNM - Barcelona SPAIN	nicolas.camara@imb-cnm.csic.es
Camarda Massimo	CNR-IMM - Catania ITALY	massimo.camarda@imm.cnr.it
Camassel Jean	GES-CNRS - Montpellier FRANCE	camasell@ges.univ-montp2.fr
Capano Mike	Purdue University, West Lafayette USA	capano@purdue.edu
Castaing Ambroise	Swansea University UNITED KINGDOM	a.castaing.495707@swansea.ac.uk
Chassagne Thierry	NOVASIC FRANCE	tchassagne@novasic.com
Coffa Salvo	ST Microelectronics - Catania ITALY	salvo.coffa@st.com
Compagnini Giuseppe	University of Catania ITALY	gcompagnini@unict.it
Condorelli Giuseppe	LPE-ETC - Catania ITALY	g.condorelli@etc-epi.com
Constant Aurore	CSIC-CNM - Barcelona SPAIN	aurore.constant@imb-cnm.csic.es
Cooke Graham	Hiden Analytical LTD UNITED KINGDOM	gcooke@hiden.co.uk
Crippa Danilo	LPE-ETC - Catania ITALY	danilo.crippa@lpe-epi.com
Delugas Pietro	CNR-IMM - Catania ITALY	pietro.delugas@imm.cnr.it
Deretzis Ioannis	Scuola Superiore – University of Catania ITALY	ioannis.deretzis@imm.cnr.it
Di Franco Salvatore	CNR-IMM - Catania ITALY	salvatore.difranco@imm.cnr.it

Doneddu Daniele	University of Wales UNITED KINGDOM	d.doneddu@wales.ac.uk
Dudley Michael	Stony Brook University USA	mdudley@notes.cc.sunysb.edu
Eriksson Jens	CNR-IMM – Catania ITALY	jens.eriksson@imm.cnr.it
Esteve Romain	ACREO AB - Kista SWEDEN	romain.esteve@acreo.se
Fallica Giorgio	ST Microelectronics - Catania ITALY	giorgio.fallica@st.com
Fedele Matteo	2M Strumenti ITALY	mfedele@2mstrumenti.com
Ferro Gabriel	LMI - Villeurbanne FRANCE	gabriel.ferro@univ-lyon1.fr
Fiorenza Patrick	CNR-IMM - Catania ITALY	patrick.fiorenza@imm.cnr.it
Foti Gaetano	University of Catania ITALY	foti.gaetano@ct.infn.it
Frisina Ferruccio	ST Microelectronics - Catania ITALY	ferruccio.frisina@st.com
Galben Irina	LMGP - Grenoble FRANCE	irina.galben@inpg.fr
Gammon Peter	University of Warwick UNITED KINGDOM	p.m.gammon@warwick.ac.uk
Germain Marianne	IMEC - Leuven Belgium	Marianne.Germain@imec.be
Giannazzo Filippo	CNR-IMM - Catania ITALY	filippo.giannazzo@imm.cnr.it
Godignon Philippe	CSIC-CNM - Barcelona SPAIN	philippe.godignon@imb- cnm.csic.es
Greco Maurizio	ST Microelectronics - Catania ITALY	maurizio.greco@st.com
Guy Owen	Swansea University UNITED KINGDOM	O.J.Guy@swansea.ac.uk
Hens Philip	University of Erlangen GERMANY	philip.hens@uni-erlangen.de
Iucolano Ferdinando	CNR-IMM Catania ITALY	ferdinando.iucolano@imm.cnr.it
Jarasiunas Kestutis	Vilnius University LITHUANIA	kestutis.jarasiunas@ff.vu.lt
Jegenyes Nikoletta	LMI - Villeurbanne FRANCE	nikoletta.jegenyes@adm.univ.lyon 1.fr
Jennings Mike	University of Warwick UNITED KINGDOM	M.R.Jennings@warwick.ac.uk
Juillaguet Sandrine	GES-CNRS - Montpellier FRANCE	sandrine.juillaguet@ges.univ- montp2.fr
Kato Masashi	Nagoya Institute of Technology JAPAN	Kato.Masashi@nitech.ac.jp
Keim Uwe	Centrotherm GERMANY	uwe.keim@centrotherm.de
Krieger Michael	University of Erlangen GERMANY	michael.krieger@physik.uni- erlangen.de
La Magna Antonino	CNR-IMM - Catania ITALY	antonino.lamagna@imm.cnr.it
La Via Francesco	CNR-IMM - Catania ITALY	francesco.lavia@imm.cnr.it
Lanzieri Claudio	Selex Sistemi ITALY	clanzieri@selex-si.com
Lien Wei Cheng	University of California, Berkeley	wclien@berkeley.edu

	USA	
Limiti Ernesto	University of Rome Tor Vergata ITALY	Limiti@ing.uniroma2.it
Litrico Grazia	University of Catania ITALY	grazia.litrico@ct.infn.it
Lo Nigro Raffaella	CNR-IMM - Catania ITALY	raffaella.lonigro@imm.cnr.it
Lodzinski Michal	University of Wales - Swansea UNITED KINGDOM	m.lodzinski.443395@swansea.ac.u k
Lorenzzi Jean Carlos	LMI - Villeurbanne FRANCE	jean.lorenzzi@univ-lyon1.fr
Madar Roland	CNRS-LMGP - Grenoble FRANCE	roland.madar@inpg.fr
Malhan Rajesh Kumar	Denso Corporation JAPAN	rajesh_k_malhan@denso.co.jp
Manolis Georgios	Vilnius University LITHUANIA	georgios.manolis@mtmi.vu.lt
Marinova Maya	Aristotle University of Thessaloniki GREECE	marinova@physics.auth.gr
Mauceri Marco	LPE-ETC - Catania ITALY	m.mauceri @etc-epi.com
Mazzillo Massimo	ST Microelectronics - Catania ITALY	massimo.mazzillo@st.com
Miccoli Cristina	ST Microelectronics - Catania ITALY	cristina.miccoli@st.com
Mucciato Raffaele	2M Strumenti ITALY	rmucciato@2mstrumenti.com
Nagasawa Hiroyuki	Hoya Corporation JAPAN	Hiroyuki_Nagasawa@sngw.rdc.ho ya.co.jp
Nipoti Roberta	CNR-IMM - Bologna ITALY	roberta.nipoti@imm.cnr.it
Nizza Francesca	CNR-IMM - Catania ITALY	francesca.nizza@imm.cnr.it
Parasole Nicolò	CNR-IMM - Catania ITALY	nicolo.parasole@imm.cnr.it
Patti Alfonso	ST Microelectronics - Catania ITALY	alfonso.patti@st.com
Pecora Antonio	LPE-ETC - Catania ITALY	a.pecora@etc-epi.com
Piluso Nicolò	CNR-IMM – Catania ITALY	nicolo.piluso@imm.cnr.it
Poggi Antonella	CNR-IMM - Bologna ITALY	antonella.poggi@imm.cnr.it
Polychroniadis Efstathios	Aristotle University of Thessaloniki GREECE	polychr@auth.gr
Portail Marc	CNRS - CRHEA - Valbonne FRANCE	mpo@crhea.cnrs.fr
Puglisi Valeria	ST Microelectronics - Catania ITALY	valeria-sst.puglisi@st.com
Raineri Vito	CNR-IMM - Catania ITALY	vito.raineri@imm.cnr.it
Rambach Martin	Centrotherm GERMANY	Martin.Rambach@centrotherm.de
Ravesi Sebastiano	ST Microelectronics - Catania ITALY	sebastiano.ravesi@st.com
Reitano Riccardo	University of Catania ITALY	Riccardo.reitano@ct.infn.it
Reshanov Sergey	ACREO AB - Kista SWEDEN	sergey.reshanov@acreo.se

Rimini Emanuele	University of Catania ITALY	emanuele.rimini@ct.infn.it
Rinaudo Salvatore	ST Microelectronics – Catania ITALY	salvatore.rinaudo@st.com
Roccaforte Fabrizio	CNR-IMM - Catania ITALY	fabrizio.roccaforte@imm.cnr.it
Roy Sebastien	CNRS - CRHEA - Valbonne FRANCE	sr@crhea.cnrs.fr
Ruggiero Alfonso	ST Microelectronics - Catania ITALY	alfonso.ruggiero@st.com
Rupp Roland	Infineon Technolgies GERMANY	roland.rupp@infineon.com
Saggio Mario	ST Microelectronics - Catania ITALY	mario.saggio@st.com
Schöner Adolf	ACREO AB - Kista SWEDEN	adolf.schoner@acreo.se
Sciuto Antonella	CNR-IMM - Catania ITALY	antonella.sciuto@imm.cnr.it
Scuderi Antonino	ST Microelectronics - Catania ITALY	antonino.scuderi@st.com
Severino Andrea	CNR-IMM - Catania ITALY	andrea.severino@imm.cnr.it
Sonde Sushant	Scuola Superiore – University of Catania ITALY	sushant.sonde@imm.cnr.it
Souzis Andrew	II-VI Incorporated USA	asouzis@ii-vi.com
Spada Aldo	CNR-IMM - Catania ITALY	aldo.spada@imm.cnr.it
Spencer Michael G.	Cornell University, Ithaca USA	spencer@ece.cornell.edu
Spetz Lloyd Anita	University of Linköping SWEDEN	spetz@ifm.liu.se
Spinella Corrado	CNR-IMM - Catania ITALY	corrado.spinella@imm.cnr.it
Stephen Saddow	University of South Florida, Tampa USA	saddow@eng.usf.edu
Strazzulla Gianni	INAF - Astrophysical Observatory Catania ITALY	gianni@oact.inaf.it
Sun Guoli	LMGP - Grenoble FRANCE	guoli.sun@minatec.inpg.fr
Sun Jianwu	GES-CNRS - Montpellier FRANCE	jianwus@yahoo.com.cn
Syvajarvi Mikael	University of Linköping SWEDEN	msy@ifm.liu.se
Tazzoli Augusto	University of Padova - DEI ITALY	augusto.tazzoli@dei.unipd.it
Tournier Dominique	Ampere INSA - LYON FRANCE	dominique.tournier@insa-lyon.fr
Trapaidze Lia	University of Erlangen GERMANY	lia_trapaidze@yahoo.com
Tsirimpis Athanaslos	University of Erlangen GERMANY	Thanos.Tsirimpis@physik.uni-erlangen.de
Vasiliauskas Remigijus	University of Linköping SWEDEN	remis@ifm.liu.se
Wagner Guenter	Institute for Crystal Growth, Berlin GERMANY	wagner@ikz-berlin.de
Watts Bernard	CNR-IMEM - Parma ITALY	watts@imem.cnr.it
Weng Ming-Hung	CNR-IMM - Catania	minghung.weng@imm.cnr.it

	ITALY	
Wischmeyer Frank	AIXTRON AG - Aachen GERMANY	wis@aitron.com
Yakimova Rositza	University of Linköping SWEDEN	roy@ifm.liu.se
Zanetti Edoardo	ST Microelectronics - Catania ITALY	edoardo.zanetti@st.com
Zanoli Laura Maria	Scuola Superiore – University of Catania ITALY	lzanoli@unict.it
Zoulis Georgios	GES-CNRS - Montpellier FRANCE	zoulis@ges.univ-montp2.fr